BECKHOFF New Automation Technology

Original manual | EN

CB7268

Computerboard

27.08.2020 | Version: 1.1

Table of contents

1 Documentation issue status

Version	Modifications
0.1	Preliminary version, mechanical part only
0.2	Preliminary version, BIOS entries added.
0.3	Preliminary version
1.0	Initial release, incl. change from BAseCon140 to BeaCon140
1.1	BIOS 0.14, updated and new cover page

2 Notes on the documentation

This description is only intended for the use of trained specialists in control and automation engineering who are familiar with the applicable national standards.
It is essential that the documentation and the following notes and explanations are followed when installing and commissioning the components.
It is the duty of the technical personnel to use the documentation published at the respective time of each installation and commissioning.

The responsible staff must ensure that the application or use of the products described satisfy all the requirements for safety, including all the relevant laws, regulations, guidelines and standards.

Disclaimer

The documentation has been prepared with care. The products described are, however, constantly under development.
We reserve the right to revise and change the documentation at any time and without prior announcement.
No claims for the modification of products that have already been supplied may be made on the basis of the data, diagrams and descriptions in this documentation.

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Patents

The EtherCAT technology is patent protected, in particular by the following applications and patents:
EP1590927, EP1789857, EP1456722, EP2137893, DE102015105702
with corresponding applications or registrations in various other countries.

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3 Safety instructions

Safety regulations

Please note the following safety instructions and explanations!
Product-specific safety instructions can be found on following pages or in the areas mounting, wiring, commissioning etc.

Exclusion of liability

All the components are supplied in particular hardware and software configurations appropriate for the application. Modifications to hardware or software configurations other than those described in the documentation are not permitted, and nullify the liability of Beckhoff Automation GmbH & Co. KG.

Personnel qualification

This description is only intended for trained specialists in control, automation and drive technology who are familiar with the applicable national standards.

Description of symbols

In this documentation the following symbols are used with an accompanying safety instruction or note. The safety instructions must be read carefully and followed without fail!

⚠ DANGER

Serious risk of injury!

Failure to follow the safety instructions associated with this symbol directly endangers the life and health of persons!

⚠ WARNING

Risk of injury!

Failure to follow the safety instructions associated with this symbol endangers the life and health of persons!

⚠ CAUTION

Personal injuries!

Failure to follow the safety instructions associated with this symbol can lead to injuries to persons!

NOTE

Damage to the environment or devices

Failure to follow the instructions associated with this symbol can lead to damage to the environment or equipment.

Tip or pointer

This symbol indicates information that contributes to better understanding.

UL note

This symbol indicates important information regarding UL certification.

Intended use

The CB7268 Computer Board was designed and developed exclusively for configuration in automation processes. To that end the board is equipped with external interfaces in order to acquire or output digital or analog signals or forward them to higher-level components.

Any other use is regarded as inappropriate.

The specified limits for electrical and technical data must be adhered to.

4 Overview

4.1 Properties

The CB7268 is a high-performance compact board, based on Intel®'s Whiskeylake processor. State-of-the-art energy-saving DDR4 technology enables memory extension up to 16 GB.

Standard interfaces include one DisplayPort connector in the front panel, 3 Gigabit LAN connectors and 4 USB3.1 GEN2 interfaces.

The BeaCon140 connector allows flexible expansion of the CB7268's I/O functions. It provides 7 PCIe lanes, of which 4 can be multiplexed with SATA signals and 3 with USB 3.1 GEN2-signals. The configuration of the I/O functions is taken care of by the PIC on the expansion card. The PIC contains the configuration data, which are communicated to the board upon connection and thus enable an uncomplicated and self-configuring extension of the I/O options.

An LED indicates the status of the power controller.

The tiny CB7268 offers the full functionality of a motherboard.

Power is supplied via a 4-pin connector on the front panel.

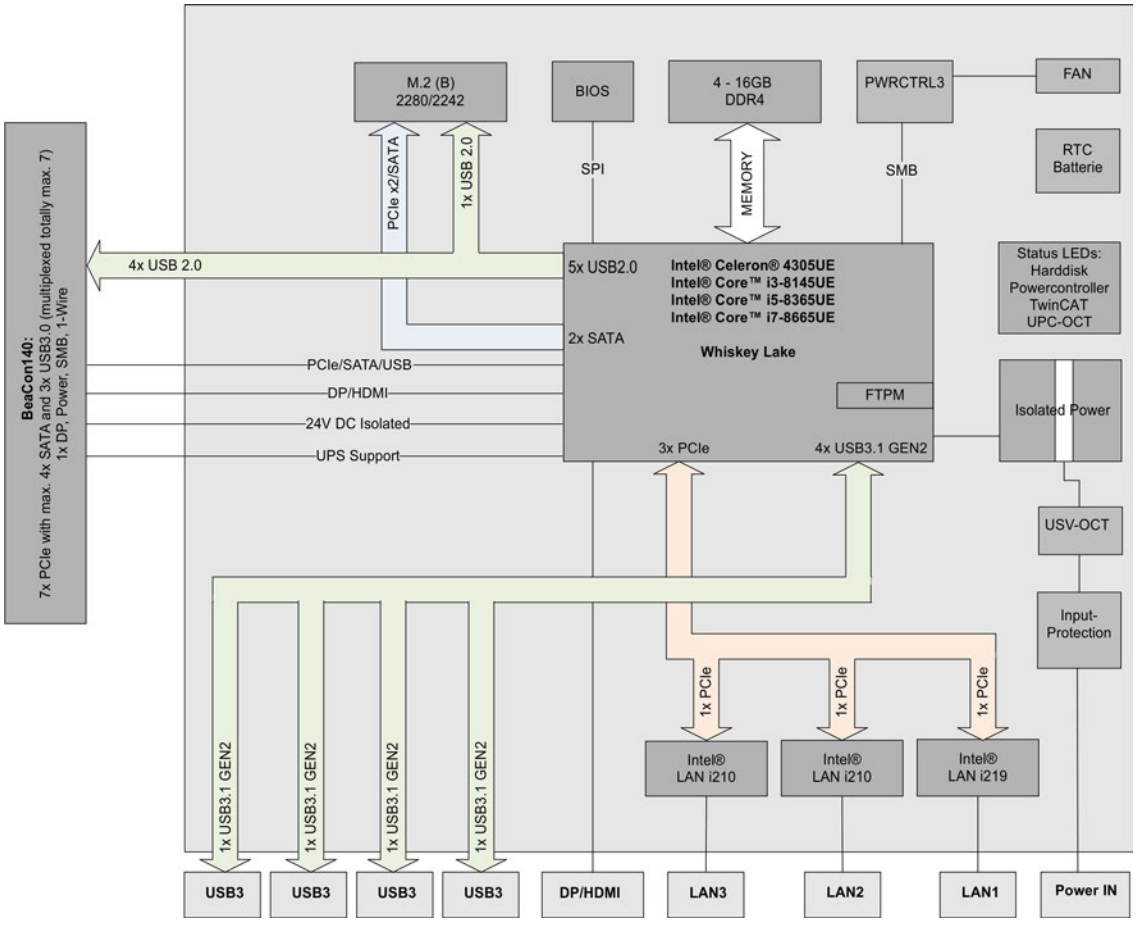


Fig. 1: CB7268 block diagram

4.2 List of features

Availability of the processors

The list of features lists all the processors that can be ordered. Their actual availability depends on the manufacturer.

List of features	
CB7268	**120 x 75 Board**
CPU	Intel® Celeron® 4305U (DC, 2M, 2.0 GHz), TDP 15 W Intel® Core™ i3-8145U (DC, 2M, 2.1 GHz), TDP 15 W Intel® Core™ i5-8365U (QC, 6M, 1.6 GHz), TDP 15 W Intel® Core™ i7-8665U (QC, 8M, 1.7 GHz), TDP 15 W
Socket	FCBGA1528
Memory	OnBoard DDR4-2400/LPDD3-2133 (depending on CPU up to 2400 MHz, up to 8 GB)
I/O on front panel	1 x power 1x DisplayPort(connection of an HDMI adapter for an HDMI signal is possible.) 3 x LAN 10/100/1000 4 x USB 3.1 GEN2
Internal I/O	1x M.2 (B) socket, signals depend on chipset (see Internal: M.2 [▶ 22] 1 x BeaCon140, signals (see Internal: BeaCon140 [▶ 18])
Graphic resolution	Max. resolution (HDMI 1.4) 4096x2304@24Hz Max. resolution (DP1.2) 4096x2304@60Hz Max. resolution (eDP - integrated flat screen) 4096x2304@60Hz
RTC	With external CMOS battery (via 2-pin connector or expansion card)
BIOS	AMI® Aptio V
Power supply	24 V_{DC} power supply unit (+20 % / - 15 %) Overvoltage and undervoltage protection Reverse polarity protection, UPS-OCT possible
Format	120 x 75 mm, electrically isolated

4.3 Specifications and documents

The following documents, specifications or webpages were used for the preparation of this manual or as further technical documentation respectively.

- **PCI Express® Base Specification**
- Version 2.0
- www.pcisig.com
- **ACPI specification**
- Version 3.0
- www.acpi.info
- **ATA/ATAPI specification**
- Version 7 Rev. 1
- www.t13.org
- **USB specifications**
- www.usb.org
- **SM-Bus specification**
- Version 2.0
- www.smbus.org
- **Intel® chip descriptions**
- Intel® WhiskeyLake product family data sheet, processors (Celeron4305UE, i3-8145UE, i5-8345UE, i7-8665UE)
- www.intel.com
- **Intel® chip description**
- i210 datasheet
- i219 data sheet
- www.intel.com
- **American Megatrends®**
- Aptio™ Text Setup Environment (TSE) User Manual
- www.ami.com
- **American Megatrends®**
- Aptio™ 5.x Status Codes
- www.ami.com

5 External connections

5.1 External connector overview

The figure shows the external interfaces of the CB7268. The following list shows the interfaces with reference to the respective manual page, where further information about the respective interface can be found.

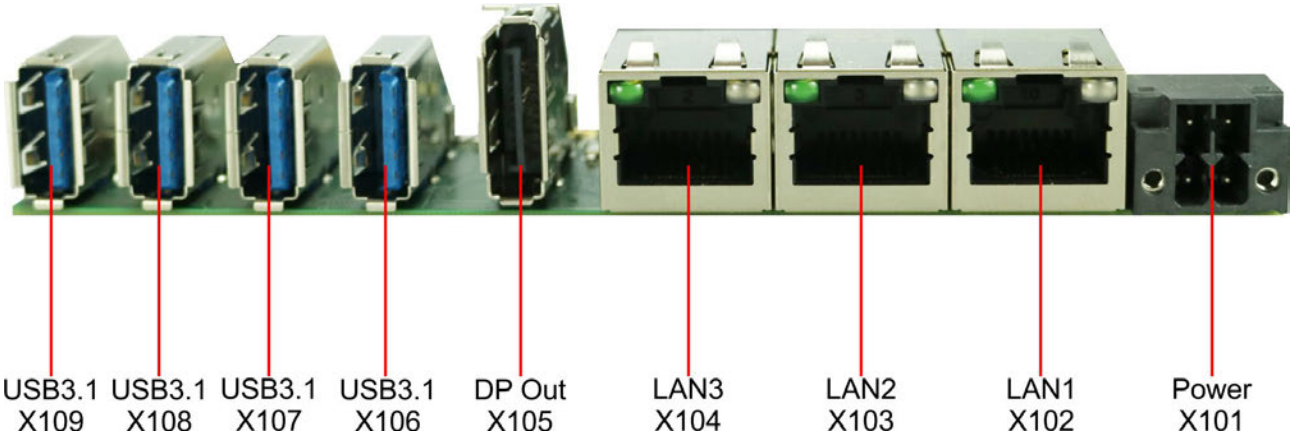


Fig. 2: CB7268, external interfaces

Front panel

The illustration corresponds to the installation situation in the PC housing.

5.2 List of interfaces

*number	Function (designation)	Page
P1300	Vin (X101)	See: Front panel: Power supply (X101) [▶ 13]
P900	LAN 1 (X102)	See: Front panel: LAN 1 - 3 (X102, X103, X104) [▶ 14]
P905	LAN 2 (X103)	See: Front panel: LAN 1 - 3 (X102, X103, X104) [▶ 14]
P902	LAN 2 (X104)	See: Front panel: LAN 1 - 3 (X102, X103, X104) [▶ 14]
P906	DisplayPort (X105)	See: Front panel: DisplayPort (X105) [▶ 15]
P901	USB3.1 (X106)	See: Front panel: USB 3.1 GEN2 (X106-X109) [▶ 16]
P903	USB3.1 (X107)	See: Front panel: USB 3.1 GEN2 (X106-X109) [▶ 16]
P904	USB3.1 (X108)	See: Front panel: USB 3.1 GEN2 (X106-X109) [▶ 16]
P907	USB3.1 (X109)	See:Front panel: USB 3.1 GEN2 (X106-X109) [▶ 16]
*Listing from right to left		

The numbers in brackets correspond to the external interfaces on the housing at the front of the Industrial PC.

5.3 Front panel: Power supply (X101)

Fig. 3: CB7268 Power X101

The connection for the power supply is implemented as a 2x2 pin housing connector (P20THR-1818504). The main power supply (24 V) for the module is on pin 3. This can also be implemented as UPS-OCT (One Cable Technology), i.e. the signal for the UPS is also transmitted to the board via this cable.

Please note that there are system states in which the activation of a connected PC_Start switch is ignored by the system, e.g. during booting of a Windows operating system.

In this case, repeat the operation of the switch after a few seconds.

The same applies to connected PC_Start push buttons.

Pin assignment of the power plug:					
Description	**Signal**	**Pin**		**Signal**	**Description**
PC_On: Input for starting and shutting down the PC. Low (0 V or open contact): PC starts. High (>3 V): PC shuts down.	PC_On	1	3	Vin	24 V supply voltage UPS-OCT is supported.
Power status: Output of the Power Status. The voltage corresponds to the positive supply voltage and can be loaded up to 500 mA. Low (0 V): PC is off. High (Vin): PC is on.	PC_ACTIVE	2	4	GND	Ground

5.4 Front panel: LAN 1 - 3 (X102, X103, X104)

The board has three Gigabit-LAN connections. (10BaseT, 100BaseT and 1000BaseT compatible network components can be connected to these. The required speed is selected automatically. Auto-Cross and Auto-Negotiate are available as well as PXE and RPL functionality. The controller is Intel®'s i219 for LAN1 and i210 for LAN 2 and LAN3.

Fig. 4: CB7268 LAN X102-104

Pin assignment of LAN connector:		
Pin	**Name**	**Description**
1	LAN-0	LAN line 0 +
2	LAN-0#	LAN line 0 -
3	LAN-1	LAN line 1 +
4	LAN-2	LAN line 2 +
5	LAN-2#	LAN line 2 -
6	LAN-1#	LAN line 1 -
7	LAN-3	LAN line 3 +
8	LAN-3#	LAN line 3 -

The LEDs of the LAN interfaces indicate the activity and speed of the data transmission (Mbit/s). The left-hand LED lights up when there is a connection and activity, and the right-hand LED during data transmission:

Left LED **Permanent with connection, Flashing during data transmission**	**Right LED** **Permanent during data transmission**	**Mbit/s**
Green	Green	1000
Green	Orange	100
Green	None	10

Real-time applications

The Ethernet port connected via PCIe is usually suitable for cycle times <= 1 ms and for distributed clock applications with EtherCAT.
The Ethernet port integrated in the chipset is usually suitable for real-time Ethernet applications with cycle times > 1 ms (without distributed clocks).

5.5 Front panel: DisplayPort (X105)

For devices with a DisplayPort connection a corresponding standard connector (Foxconn 3VD11203-DPA1-4H) with one DisplayPort connection is available.

The interface additionally provides HDMI/DVI signals that can be used with aid of an adapter. Please consult your distributor with regard to a suitable adapter.

Fig. 5: CB7268 DP Out X105

Pin assignment of DisplayPort plug:					
Description	**Signal**	**Pin**		**Signal**	**Description**
Display Port Lane 0 +	L0	1	2	GND	Ground
Display Port Lane 0 -	L#0	3	4	L1	Display Port Lane 1 +
Ground	GND	5	6	L#1	Line 1 -
Display Port Lane 2 +	L2	7	8	GND	Ground
Display Port Lane 2 -	L#2	9	10	L3	Display Port Lane 3 +
Ground	GND	11	12	L#3	Display Port Lane 3 -
DP / HDMI	HDMI#	13	14	GND	Ground
Auxiliary plus	AUX	15	16	GND	Ground
Auxiliary minus	AUX#	17	18	HPD	Hot Plug Detect
Ground	GND	19	20	3.3 V	Supply voltage 3.3 V

Switching to HDMI

DisplayPort signals are led out via the interface by default. With the use of a level shifter cable the board switches the DisplayPort specification 1.1 automatically to HDMI signals.

5.6 Front panel: USB 3.1 GEN2 (X106-X109)

The USB channels 1, 2, 3 and 4 are made available via a standard USB connector.

These USB channels support the 3.1-GEN2 USB specification. In contrast to the specification, the USB 3.1 channels only supply current up to 500 mA. Devices with their own current supply must be used for higher power demands. The USB interfaces are electronically protected.

All necessary settings for USB can be made in the BIOS. This applies to the USB interfaces. Note that the "USB mouse and keyboard" function in the BIOS setup is only required if the operating system does not offer USB support. This function should not be selected for settings in the setup and for booting Windows with a USB mouse and keyboard connected, because this would lead to considerable performance limitations.

Fig. 6: CB7268 USB3.1 X106-109

Pin assignment USB3.1 Gen2 connector:		
Pin	**Signal**	**Description**
1	VCC	5 V supply voltage
2	D-	Data - (USB 2.0)
3	D+	Data + (USB 2.0)
4	GND	Ground
5	RX-	Receive line - (USB 3.1)
6	RX+	Receive line + (USB 3.1)
7	GND	Ground
8	TX-	Transmit line - (USB 3.1)
9	TX+	Transmit line + (USB 3.1)

6 Internal connections

6.1 Internal connector overview

The figure shows the internal interfaces of the CB7268. The following list shows the internal connectors with reference to the respective manual page, where further information about the respective connector can be found.

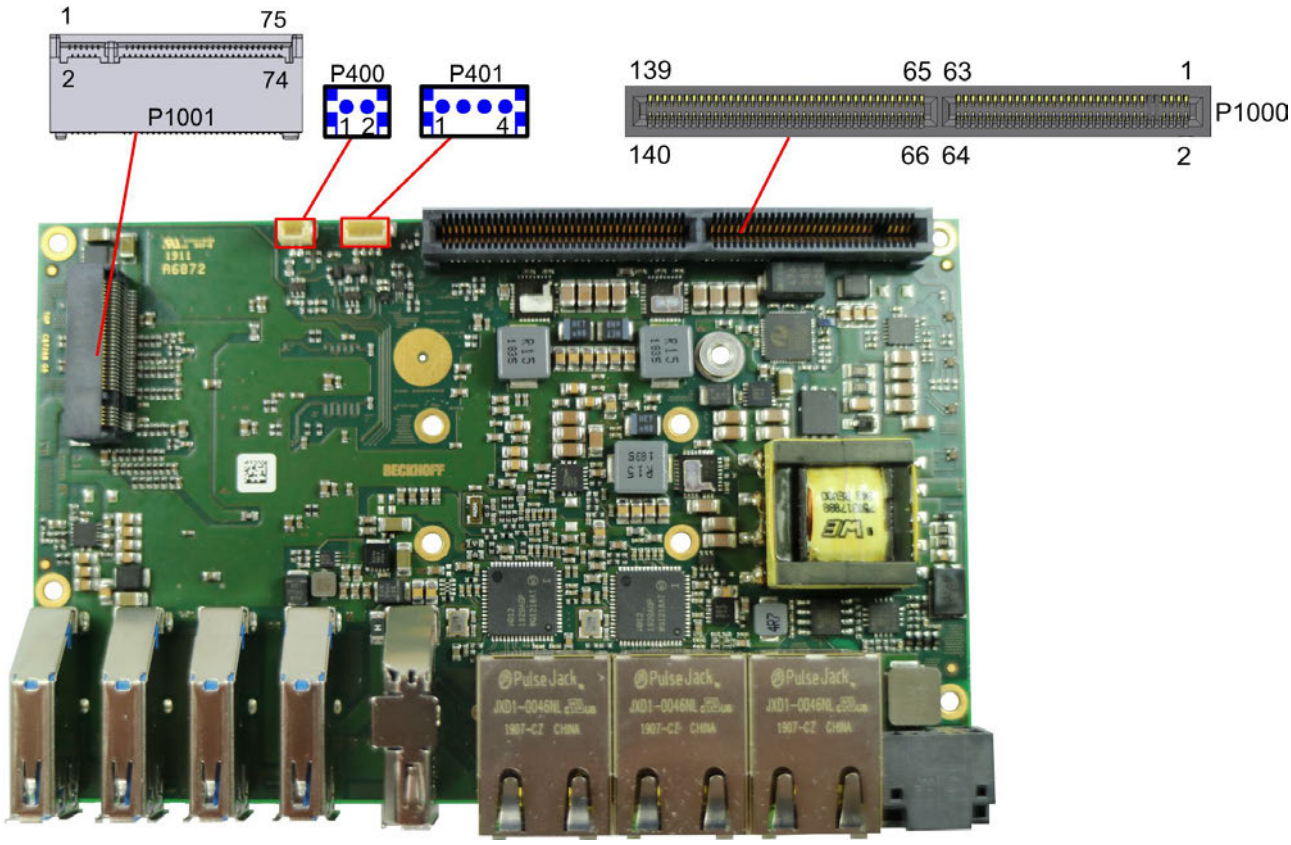


Fig. 7: CB7268 internal connector overview

6.2 List of plugs

Number	Function (designation)	Page
P1000	BeaCon140	See: Internal: BeaCon140 [▶ 18]
P401	Fan connector Housing plug (four-pin)	See: Internal: FAN [▶ 21]
P400	RealTimeClock RTC- Housing plug (two-pin)	See: Internal: Battery [▶ 21]
P1001	M.2 base (B)	See: Internal: M.2 [▶ 22]
*Listing from right to left		

6.3 Internal: BeaCon140

In conjunction with the chipset, the BeaCon140 connector allows flexible extension of the CB7268's I/O functions. It provides up to 7 PCIe lanes, of which a maximum of 4 can be multiplexed with SATA3.0 (6G) and a maximum of 4 with PCIe lines, as well as a maximum of 3 PCIe lines with a maximum of 3 USB3.1-GEN2 lines (see table). DisplayPort, SSIC, SMBus and 1-Wire signals can be fed out via the BeaCon140 connector. The extension board takes care of the configuration of the IO functions. A PIC on the expansion card contains the configuration data, which are communicated to the board upon connection and thus enable an uncomplicated and self-configuring extension of the I/O options.

Observe the current limits!

In order to avoid damaging the device, it is essential to observe the following current limits:

A maximum load of 2.8 A per pin must not be exceeded. On account of the different current consumptions of the usable processors the actual current consumption may be lower. The respective maximum values can be obtained from your distributor on inquiry.

Irrespective of the CPU in use, a maximum total load of 100 W must not be exceeded.

NOTE

Signal mirroring with BeaCon Stack Up connector

With the Stack Up version of the BeaCon connector (connector at the top of the board), a stack is used for signal transfer to the mating connector. The signals are mirrored on this mating connector (Stack Down). There is no reflection on the stack.

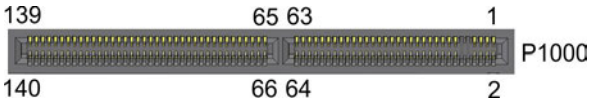


Fig. 8: CB7268-G2-BeaCon

Pin assignment of BeaCon140 connector:					
Description	**Signal**	**Pin**		**Signal**	**Description**
P_VLoad 24 V S UPS output	VOLOAD/ P_VOLOAD1	1	2	P_VIN1/VIN1	V_IN S UPS input
P_VLoad 24 V S UPS output	VOLOAD/ P_VOLOAD2	3	4	P_VIN2/VIN2	P_VIN S UPS input
(not led out)	5V/NC	5	6	P_GND/GND	Ground
(not led out)	5V/NC	7	8	P_GND/GND	Ground
	INSULATION				
Standby 5 Volt	S5V	13	14	S3.3 V	Standby 3.3 V
Ground	GND	15	16	GND	Ground
PCIe Lane 1 Transmit +	PE1/SATA4-TX	17	18	RX-SATA4/PE1	PCIe Lane 1 Receive +
PCIe Lane 1 Transmit -	PE1/SATA4-TX#	19	20	RX-SATA4/PE1#	PCIe Lane 1 Receive -
Ground	GND	21	22	GND	Ground
PCIe Clock Lane 1 +	PECLK1	23	24	PECLK2	PCIe Clock Lane 2 +
PCIe Clock Lane 1 -	PECLK1#	25	26	PECLK2#	PCIe Clock Lane 2 -
Ground	GND	27	28	GND	Ground
PCI Lane 2 Transmit +	PE2/SATA3-TX	29	30	RX-SATA3/PE2	PCIe Lane 2 Receive
PCI Lane 2 Transmit -	PE2/SATA3-TX#	31	32	RX-SATA3/PE2#	PCIe Lane 2 Receive -
Ground	GND	33	34	GND	Ground
PCIe Lane 3 Transmit +	PE3/SATA2-TX	35	36	RX-SATA2/PE3	PCIe Lane 3 Receive +
PCIe Lane 3 Transmit -	PE3/SATA2-TX#	37	38	RX-SATA2/PE3#	PCIe Lane 3 Receive -
Ground	GND	39	40	GND	Ground
PCIe Lane 3 Clock +	PECLK3	41	42	PECLK4	PCIe Clock 4 +
PCIe Lane 3 Clock 3 -	PECLK3#	43	44	PECLK4#	PCIe Clock 4 -
Ground	GND	45	46	GND	Ground
PCIe Lane 4 Transmit +	PE4/SATA1-TX	47	48	RX-SATA1/PE4	PCIe Lane 4 Receive +
PCIe Lane 4 Transmit -	PE4/SATA1-TX#	49	50	RX-SATA1/PE4#	PCIe Lane 4 Receive -
Ground	GND	51	52	GND	Ground
PCIe Clock Enable Lane 1 active low	PCKE1/DEVSLP4#	53	54	DEVSLP3/PCKE2#	PCIe Lane 2 Clock Enable active low
PCIe Clock Enable Lane 3 -	PCKE3/DEVSLP2#	55	56	DEVSLP1/PCKE4#	PCIe Lane 4 Clock Enable -
PCIe Reset active low	PERST#	57	58	PEWAKE#	PCIe Wake active low
SMBus Clock	SMBCLK	59	60	SMBDAT	SMBus Data
	KEY				
SMBus Alert active low	SMB-Alert#	61	62	1Wire	1-Wire
PCIe Clock Enable Lane 5	PCKE5/OC4#	63	64	OC3/PCKE6#	PCIe Lane 6 Clock Enable 6 -
	KEY				
PCIe Clock Enable Lane 7	PCKE7/OC2#	65	66	OC1/PCKE8#	USB Overcurrent active low
Ground	GND	67	68	GND	Ground
PCIe Lane 5 Transmit +	PE5/USB3-4/ USBC1-TX	69	70	RX-USBC1/ USB3-4/PE5	PCIe Lane 5 Receive +
PCIe Lane 5 Transmit -	PE5/USB3-4/ USBC1-TX#	71	72	RX-USBC1/ USB3-4/PE5#	PCIe Lane 5 Receive -

Pin assignment of BeaCon140 connector:					
Description	**Signal**	**Pin**		**Signal**	**Description**
USB 2.0 Channel 7 +	USB2-4#/(GND)	73	74	USB2-3/(GND)	USB 2.0 channel 8 Data +
PCIe Clock Lane 5 +	PECLK5/ USBC-SBU1/ (GND)	75	76	PECLK6/(GND)	PCIe Lane 6 Clock +
PCIe Clock 5 -	PECLK5/ USBC-SBU2#/ (GND)	77	78	PECLK6#/(GND)	PCIe Clock Lane 6 -
USB 2.0 Channel 7 -	USB2-4#/(GND)	79	80	USB2-3 D#/(GND)	USB 2.0 channel 8
(not led out)	PE6/USB3-3/ USBC2-TX	81	82	RX-USBC2/ USB3-3/PE6	(not led out)
(not led out)	PE6/USB3-3-TX/ USBC2-TX#	83	84	RX-USBC2/ USB3-3/PE6#	(not led out)
Ground	GND	85	86	GND	Ground
PCIe Lane 7 Transmit +	PE7/USB3-2-TX	87	88	RX-USB3-2/PE7	PCIe Lane 7 Receive +
PCIe Lane 7 Transmit -	PE7/USB3-2-TX#	89	90	RX-USB3-2/PE7#	PCIe Lane 7 Receive -
USB 2.0 Channel 9 +	USB2-2 (GND)	91	92	USB2-1/(GND)	USB 2.0 Channel 10 +
PCIe Lane 8 Transmit +	PECLK7/(GND)	93	94	PECLK8/(GND)	PCIe Lane 8 Clock +
PCIe Lane 8 Transmit -	PECLK7#/(GND)	95	96	PECLK8#/(GND)	PCIe Clock Lane 8 -
USB 2.0 Channel 9 -	USB2-2#/(GND)	97	98	USB2-1#/(GND)	USB 2.0 Channel 10 -
PCIe Lane 8 Transmit +	PE8/USB3-1-TX	99	100	RX-USB3-1/PE8	PCIe Lane 8 Receive +
PCIe Lane 8 Transmit -	PE8/USB3-1-TX#	101	102	RX-USB3-1/PE8#	PCIe Lane 8 Receive -
Ground	GND	103	104	GND	Ground
KEY					
SATA GP1	SATAGP1	105	106	SATAGP2	SATA GP 2
(not led out)	SATAGP3/ USBC-CC1	107	108	USB-CC2/ SATAGP4/	(not led out)
TwinCAT LED Red	TCLEDR	109	110	TCLEDG	TwinCAT LED Green
TwinCAT LED Blue	TCLEDB	111	112	RES	LAN-Sync
SATA LED active low	SATA-LED	113	114	USBPWREN	USB Power Enable
RTC Battery	BATT	115	116	PWRFAIL	SUSV
Power Management Event active low	PME#	117	118	PWRGOOD	Power good
Power button active low	PWRBTN#	119	120	MRST#	Reset button active low
PSON	PSON	121	122	ATXPWRGD	ATX Power good
Ground	GND	123	124	GND	Ground
DisplayPort -/ HDMID	DP#/DVI	125	126	DDCC/ DPAUX	DDC Clock / DisplayPort Aux +
DisplayPort Hot Plug Detect	DPHPD	127	128	DDCD/ DPAUX#	DDC Data / DisplayPort Aux -
Ground	GND	129	130	GND	Ground
DisplayPort Lane 0 +	DPL0/TMDSD2	131	132	TMDSD1/DPL1	DisplayPort Lane 1+
DisplayPort Lane 0 -	DPL0/TMDSD2#	133	134	TMDSD1DPL1#	DisplayPort Lane 1 -
Ground	GND	135	136	GND	Ground
DisplayPort Lane 2+	DPL2/TMDS0	137	138	TMDSD3/DPL3	DisplayPort Lane 3 +
DisplayPort Lane 2 -	DPL2/FMDS0#	139	140	TMDSD3/DPL3#	DisplayPort Lane 3 -

6.4 Internal: Battery

The computer board has a two-pin battery connector. This allows an RTC battery to be connected directly to the computer board.

Fig. 9: CB7268-G2-Bat

Pin assignment: Battery connector		
Pin	**Signal**	**Description**
1	3.3 V_RTC	3.3 V for RTC of the CPU
2	GND	Ground

6.5 Internal: FAN

The computer board has a four-pin fan connector. This allows fans with 12 V supply voltage to be connected directly to the computer board. A signal for monitoring the fan speed is also available.

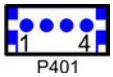


Fig. 10: CB7268-G2-Fan

Pin assignment of fan connector:		
Pin	**Signal**	**Description**
1	GND	Ground
2	12 V	Supply voltage 12 V regulated
3	TACHO	Speed monitoring
4	PWM	Speed control

6.6 Internal: M.2

The CB7268 is equipped with an M.2 socket (KeyB) into which an M.2-2280 card or M.2-2242 card (Key B) can be inserted. Adapter cards with standard plug connectors are available as accessories. Please contact your distributor for this.

Fig. 11: CB7268-M.2

Pin assignment M.2 connector (Key B)					
Description	**Signal**	**Pin**		**Signal**	**Description**
Configuration pin	CONFIG_3	1	2	3.3 V1	Standby S3.3 Volt
Ground	GND	3	4	3.3 V2	Standby S3.3 Volt
Ground	GND	5	6	FCPWROFF#	Full Card Power OFF active low
USB data +	USB D+	7	8	WDISABLE#	(not led out)
USB data -	USB D-	9	10	GPIO9/DAS/ DDS/LED1	(not led out)
Ground	GND	11	12	Connector Key	
Connector Key		13	14		
		15	16		
		17	18		
		19	20	GPIO5	(not led out)
Configuration pin	Config 0	21	22	GPIO6	(not led out)
(not led out)	GPIO11	23	24	GPIO7	(not led out)
(not led out)	DPR	25	26	GPIO10	(not led out)
Ground	GND	27	28	GPIO8	(not led out)
PCIe Lane 2 Receive -	PER1-USB3RX-SSICRX#	29	30	UIM RST	(not led out)
PCIe Lane 2 Receive +	PER1-USB3RX-SSICRX	31	32	UIM CLK	(not led out)
Ground	GND	33	34	UIM DATA	(not led out)
PCIe Lane 2 Transmit -	PET1-USB3TX-SSICTX#	35	36	UIM PWR	(not led out)
PCIe Lane 2 Transmit +	PET1-USB3TX-SSICTX	37	38	DEVSLP	DeviceSleep
Ground	GND	39	40	GPIO0	(not led out)
PCIe Lane 1 Receive +	PER0-SATAB	41	42	GPIO1	(not led out)
PCIe Lane 1 Receive -	PER0-SATAB#	43	44	GPIO2	(not led out)
Ground	GND	45	46	GPIO3	(not led out)
PCIe Lane 1 Transmit -	PET0-SATAA#	47	48	GPIO4	(not led out)
PCIe Lane 1 Transmit +	PET-SATAA	49	50	PRST#	PCIe Reset active low
Ground	GND	51	52	CLKREQ#	PCIe Clock Enable active low
PCIe Lane 1 Reference Clock -	REFCLK#	53	54	PEWAKE#	Link Reactivation active low
PCIe Lane 1 Reference Clock +	REFCLK	55	56	N/C	(not led out)
Ground	GND	57	58	N/C	(not led out)
(not led out)	ANTCTL0	59	60	COEX3	(not led out)
(not led out)	ANTCTL1	61	62	COEX2	(not led out)
(not led out)	ANTCTL2	63	64	COEX1	(not led out)
(not led out)	ANTCTL3	65	66	SIM DETECT	(not led out)
Power good	RESET#	67	68	SUSCLK	System clock
Configuration pin	CFG1	69	70	3.3 V	Standby S3.3 Volt
Ground	GND	71	72	3.3 V	Standby S3.3 Volt
Ground	GND	73	74	3.3 V	Standby S3.3 Volt
Configuration pin	CFG2	75			

7 LEDs

7.1 Power control

There is an RGB LED on the board with which status messages of the power controller are output by means of colors and flashing intervals.

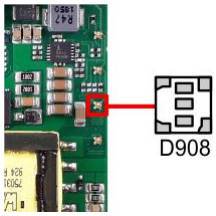


Fig. 12: CB7268 Power LED

Color	Interval	Meaning
None	Steadily lit	System in error state
White	Steadily lit	Power fail
Cyan	Steadily lit	Reserved
Magenta	Steadily lit	S UPS active (if existent)
Blue	Steadily lit	Reserved
Yellow	Steadily lit	S5 state
Green	Steadily lit	S0 state
Red	Steadily lit	Reset/Start
Green/yellow	Flashing	Bootloader running without error
Red/yellow	Flashing	Bootloader is starting (start sequence is being run through)
Yellow	Flashing (6 s)	S4 state
Yellow	Flashing (3 s)	S3 state
Magenta	Flashing (0.5 s)	S UPS capacitance test (if S UPS exists)
Red/magenta	Flashing	Checksum error during I^2C transmission in the boot loader

A steadily lit red LED can indicate a hardware error.

Adaptation of the status codes

It is possible to adapt the status codes (e.g. as TwinCAT LED). To do this, the system colors can be changed with the aid of an SMB command. This change remains in force until the next restart or reset. A change of the default colors is indicated by the additional flashing of the white LED.

7.2 SATA

The RGB LED indicates the hard disk activity.

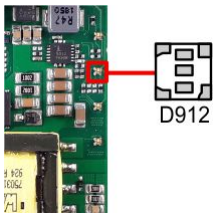


Fig. 13: CB7268 SATA LED

Color	Interval	Meaning
Red	Flashing	Activity (access)

7.3 TwinCAT

This RGB LED indicated the status of TwinCAT activity.

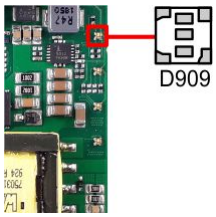


Fig. 14: CB7268 TC LED

Color	Interval	Meaning
Green	Steadily lit	TwinCAT Run Mode
Blue	Steadily lit	TwinCAT Config Mode
Red	Steadily lit	TwinCAT Stop

7.4 UPS-OCT

An RGB LED on the board indicates the status of the OCT interface via colors and flashing intervals.

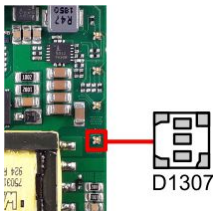


Fig. 15: CB7268 OCT LED

Color	Interval	Meaning
None	Steadily lit	No UPS-OCT connected
Blue	Flashing	Boot loader active
Yellow	Flashing	Moderate signal quality
Green	Flashing	Good signal quality
Red	Flashing	Poor signal quality

If the LED is not lit, no UPS-OCT is connected.

Adaptation of the status codes

It is possible to adapt the status codes (e.g. as UPS-OCT-LED). To do this, the system colors can be changed with the aid of an SMB command. This change remains in force until the next restart or reset.

8 BIOS

8.1 Using the setup

Within the individual setup pages the last saved settings can be restored can at any time with F2 (”Previous Values”). Use F3 (”Optimized Defaults”) to load the factory defaults. Use F2/F3 to load the complete set of settings and F4 to save them (”Save & Exit").

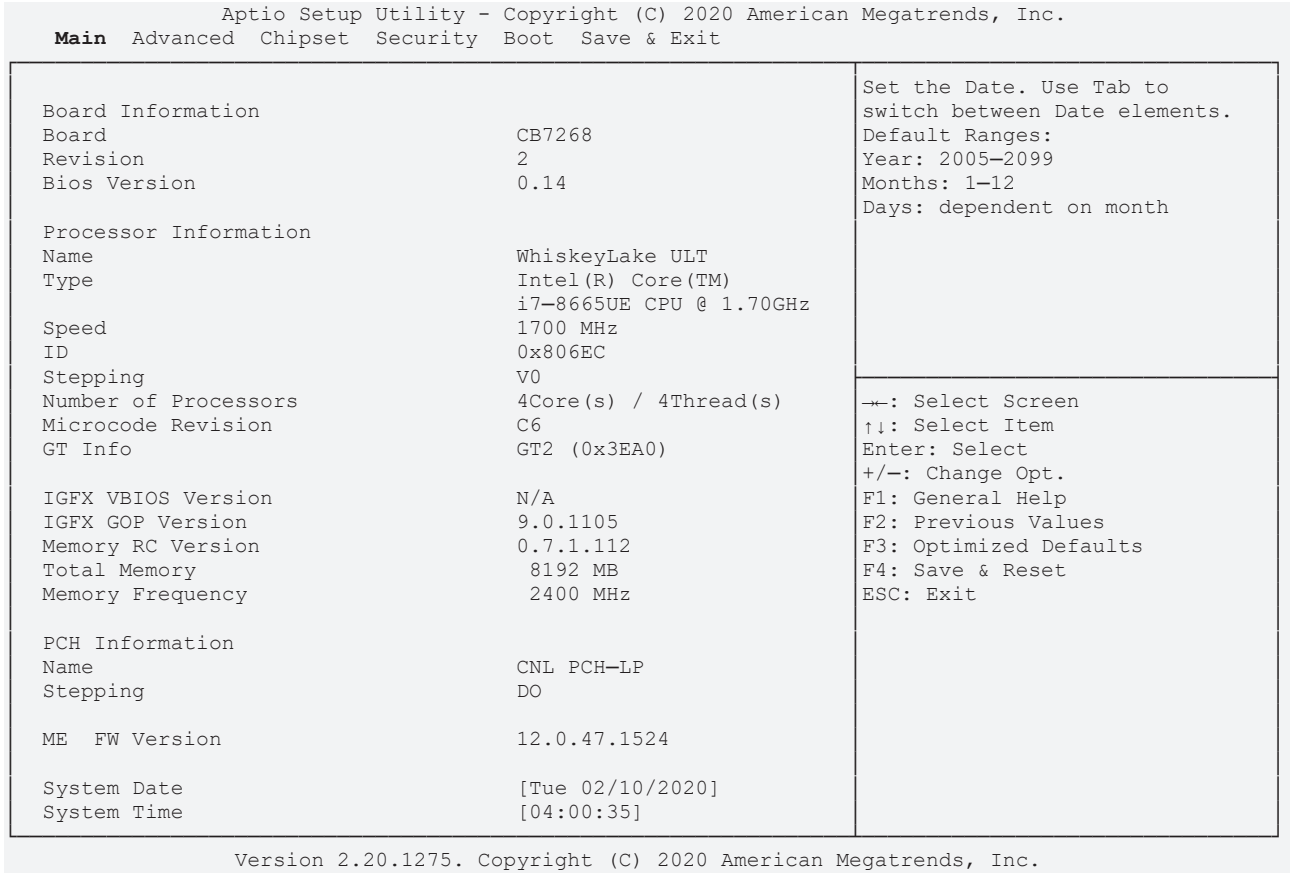
A “►” sign in front of the menu item indicates that a submenu is available. Use the arrow keys to navigate between menu items. Use the Enter key to select menu items and call submenus or selection dialogs.

For each setup option a help text is displayed at the top right, which in many cases contains useful information about the option and permitted values, etc.

Note on Setup Documentation

The BIOS is regularly updated so that the available setup options can change at any time without notice. This may result in differences between the options actually available and those described below. It should also be noted that the settings shown in the setup menus below are not necessarily the recommended or default settings. Which settings must be selected depends on the application scenario in which the board is operated.

8.2 Main



BIOS entry	Option
Board information	
Board	None
Revision	None
Bios version	None
Processor Information	
Name	None
Type	None
Speed*	None
ID	None
Stepping	None
Number of processors	None
Microcode revision	None
GT info	None
IGFX VBIOS version	None
IGFX GOP version	None
Memory RC version	None
Total Memory	None
Memory frequency	None
PCH information	
Name	None
Stepping	None
ME FW version	None
System Date	Here you can change the system date.
System Time	Here you can change the system time.

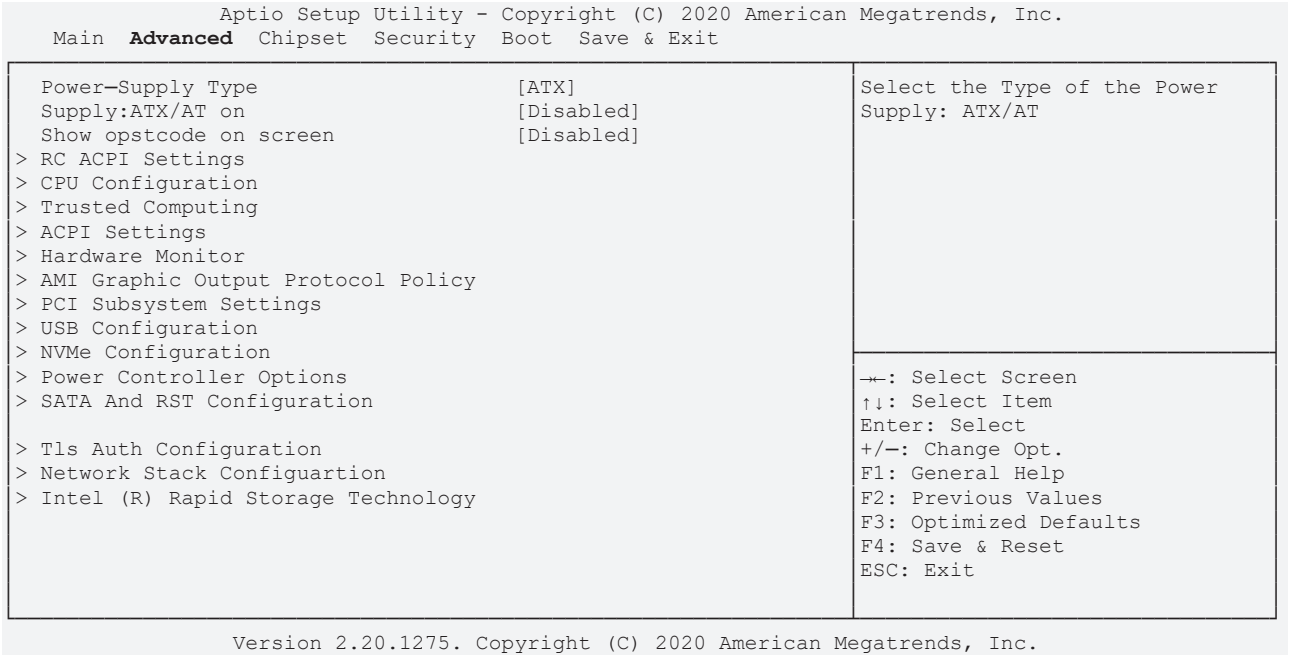
NOTE

***Speed**

All Intel® processors have a certain base frequency and a specific TDP.

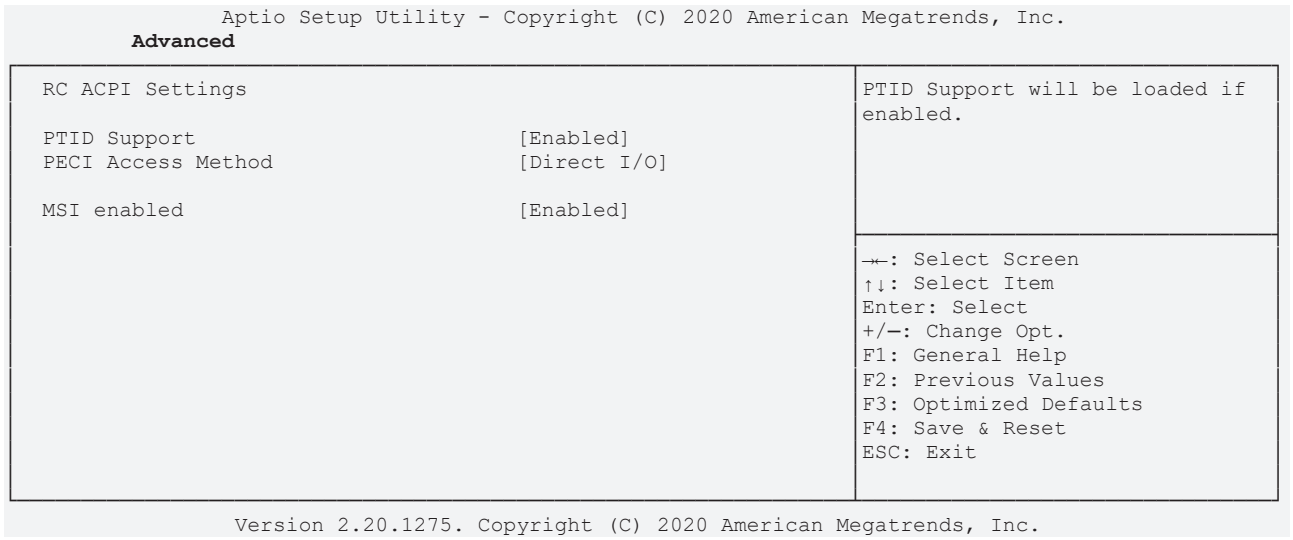
Configurable TDP options mean that the computer manufacturer can change the base frequency and TDP of the CPU within the specific values published on the product specification page at https://Ark.Intel.com.

8.3 Advanced



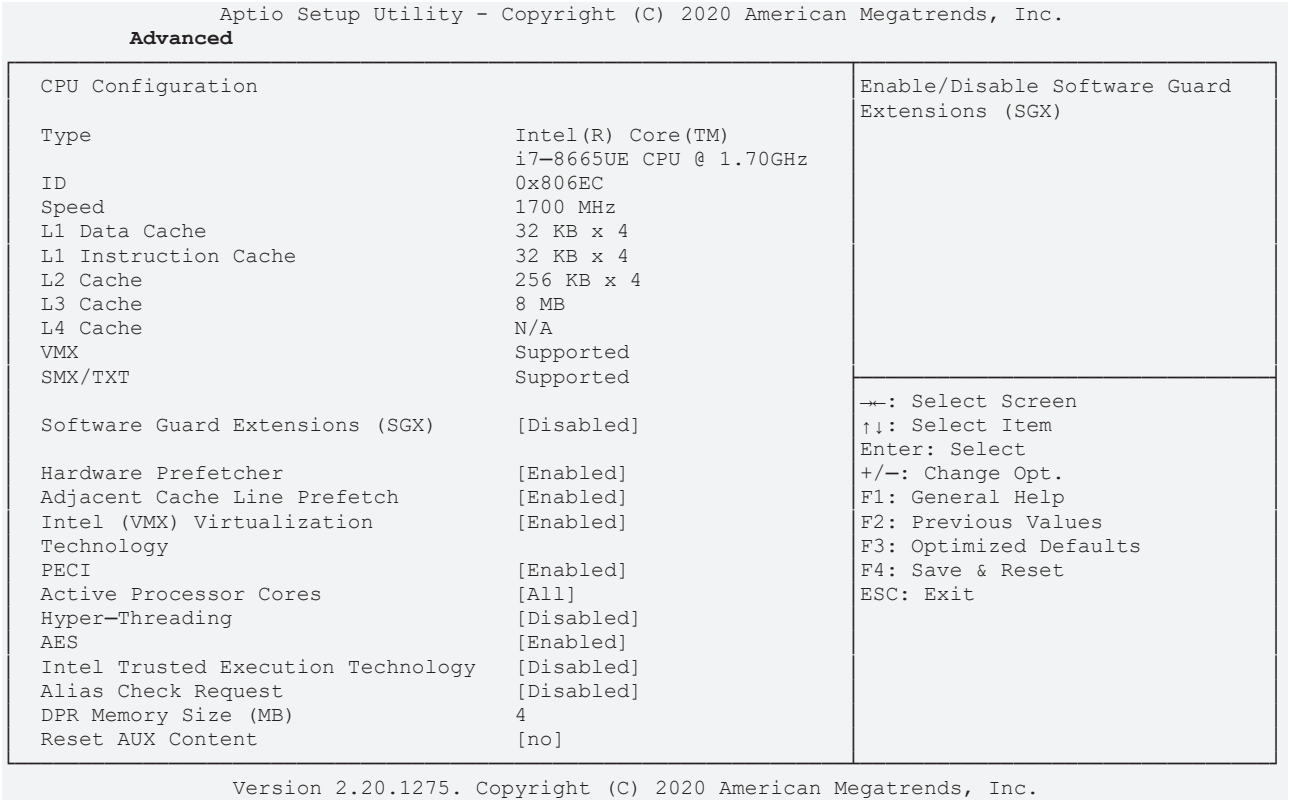
BIOS entry	Option
Power-Supply Type	[ATX/AT]
SoftOff on overheat	Disabled / Enabled / Enabled (Emulate PwrBtn)
Show postcode on screen	Disabled / Enabled
RC ACPI settings	Submenu see: RC ACPI settings [▶ 31]
CPU Configuration	Submenu see: CPU Configuration [▶ 32]
Trusted Computing	Submenu see: Trusted Computing Disable [▶ 33]
	Submenu see: Trusted Computing Enable [▶ 34]
ACPI Settings	Submenu see: ACPI Settings [▶ 35]
Hardware Monitor	Submenu see: Hardware Monitor [▶ 36]
AMI Graphic Output Protocol Policy	Submenu see: Graphic Output Protocol Policy [▶ 37]
PCI Subsystem Settings	Submenu see: PCI Subsystem Settings [▶ 37]
USB Configuration	Submenu see: USB Configuration [▶ 39]
NVMe Configuration	Submenu see: NVMe Configuration [▶ 40]
Power Controller Options	Submenu see: Power Controller Options [▶ 41]
BAseCon Configuration*	
SATA And RST Configuration	Submenu see: SATA And RST Configuration [▶ 43]
Tls Auth configuration	Submenu see: TLS Auth configuration [▶ 46]
Network Stack Configuration	Submenu see: Network Stack Configuration [▶ 47]
	Submenu see: Network stack configuration enabled [▶ 48]
Intel ® Rapid Storage Technology	Submenu see: Intel® Rapid Storage Technology [▶ 49]
Intel ® Ethernet connection(2) I219-LM - 00:01:05:4E:97:84	

8.3.1 RC ACPI settings



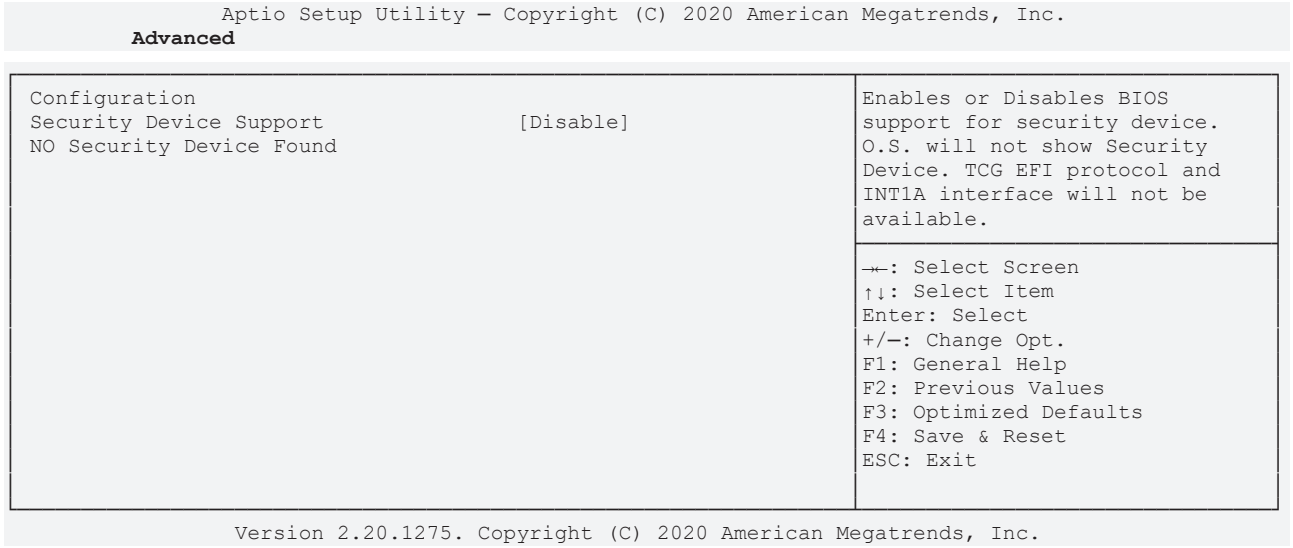
BIOS entry	Options
RC ACPI settings	
PTID support	Enabled / Disabled
PECI access method	Direct I/O / ACPI
MSI enabled	Enabled / Disabled

8.3.2 CPU Configuration



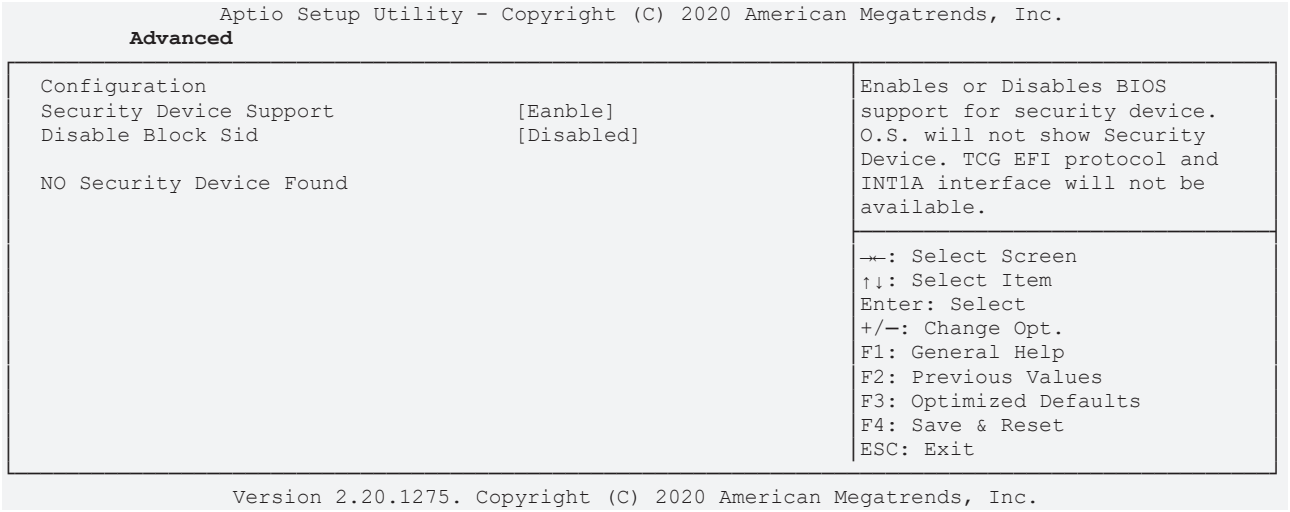
BIOS entry	Options
CPU Configuration	
Type	None
ID	None
Speed	None
L1 Data Cache	None
L1 instruction cache	None
L2 Cache	None
L3 Cache	None
L4 cache	None
VMX	None
SMX/TXT	None
Software Guard Extensions (SGX)	Disabled / Enabled / Software Controlled
Hardware prefetcher	Enabled / Disabled
Adjacent Cache Line Prefetch	Enabled / Disabled
Intel (VMX) Virtualization Technology	Enabled / Disabled
PECI	Enabled / Disabled
Active Processor Cores	All / 1 / 2 / 3
AES	Enabled / Disabled
Intel Trusted Execution Technology	None
Alias check request	None
DPR memory size (MB)	None
Reset AUX content	None

8.3.3 Trusted Computing Disable



BIOS entry	Options
Configuration	
Security device support	Disable / Enable
No security device found	

8.3.4 Trusted Computing Enable



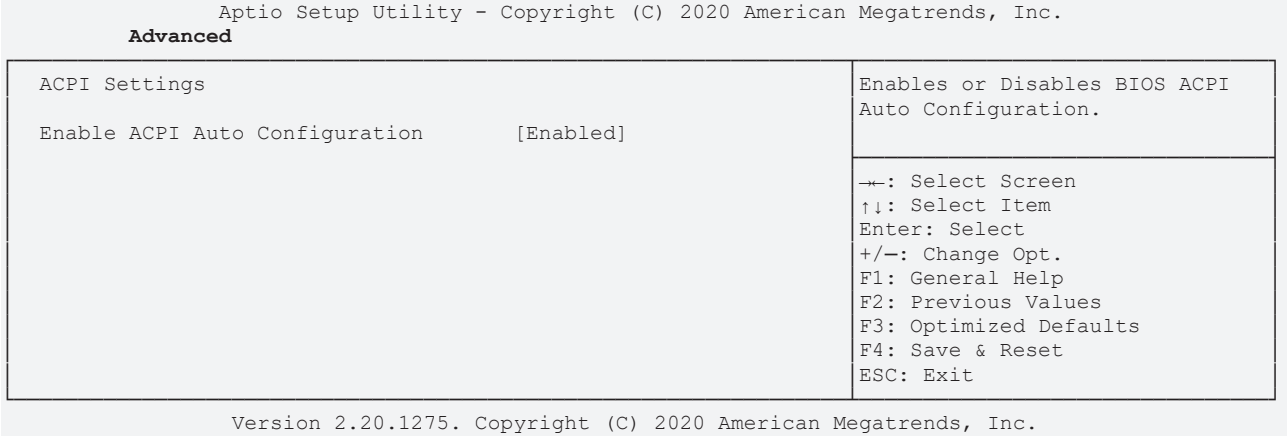
BIOS entry	Options
Configuration	
Security device support	Enable / Disable
Disable block Sid	Disabled / Enabled
No security device found	

NOTE

Activating the Enable settings

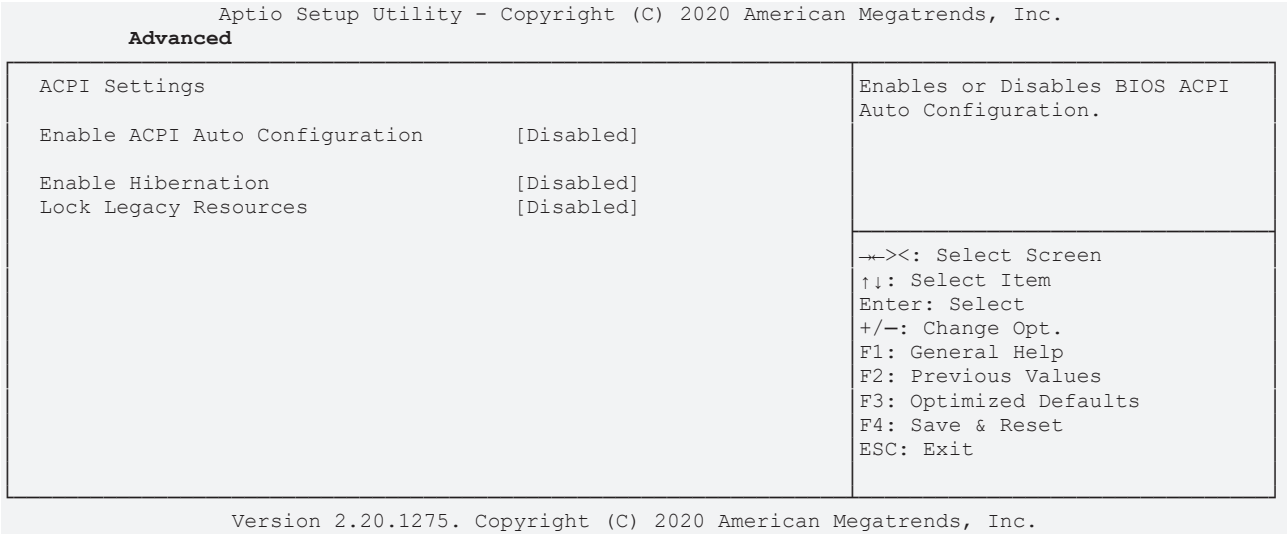
Use "Quit without saving" followed by "Yes" to perform a reset and activate the settings. Please note that not all CPUs support this function.

8.3.5 ACPI Settings Enabled



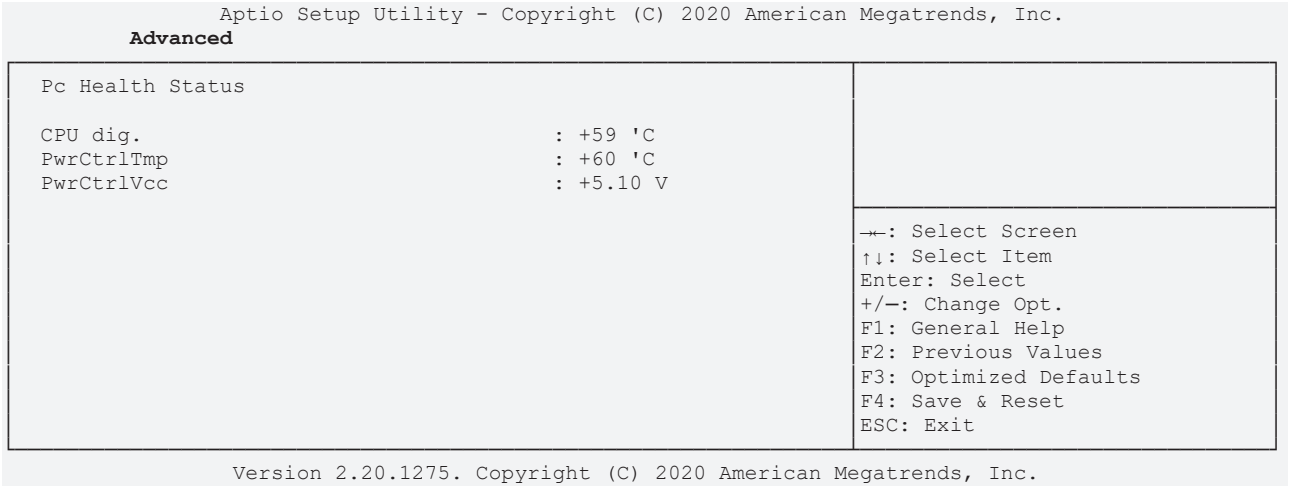
BIOS entry	Options
ACPI Settings	
Enable ACPI Auto Configuration	Enabled / Disabled

8.3.6 ACPI Settings Disabled



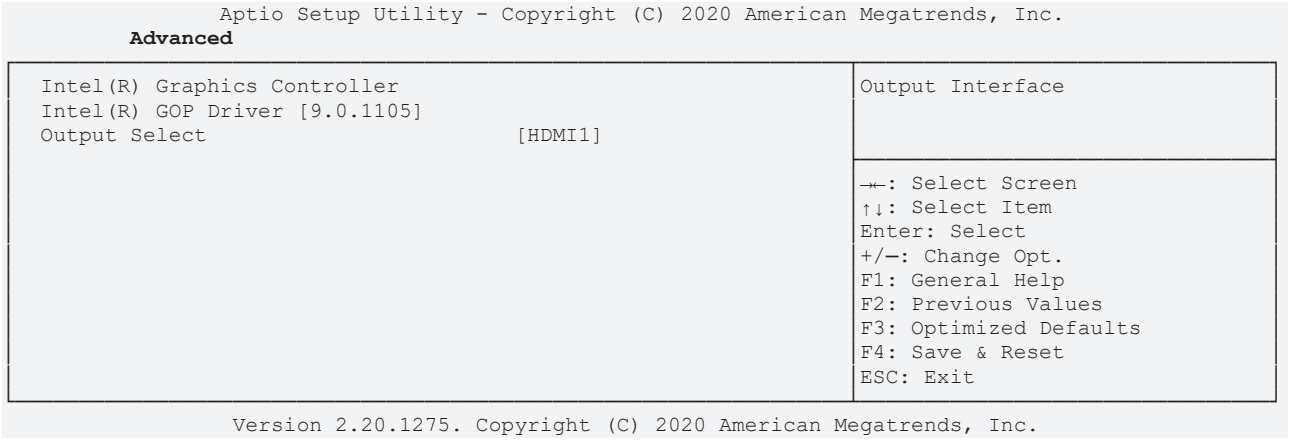
BIOS entry	Options
ACPI Settings	
Enable ACPI Auto Configuration	Disabled / Enabled
Enable hibernation	Enabled / Disabled
Lock legacy resources	Disabled / Enabled

8.3.7 Hardware Monitor



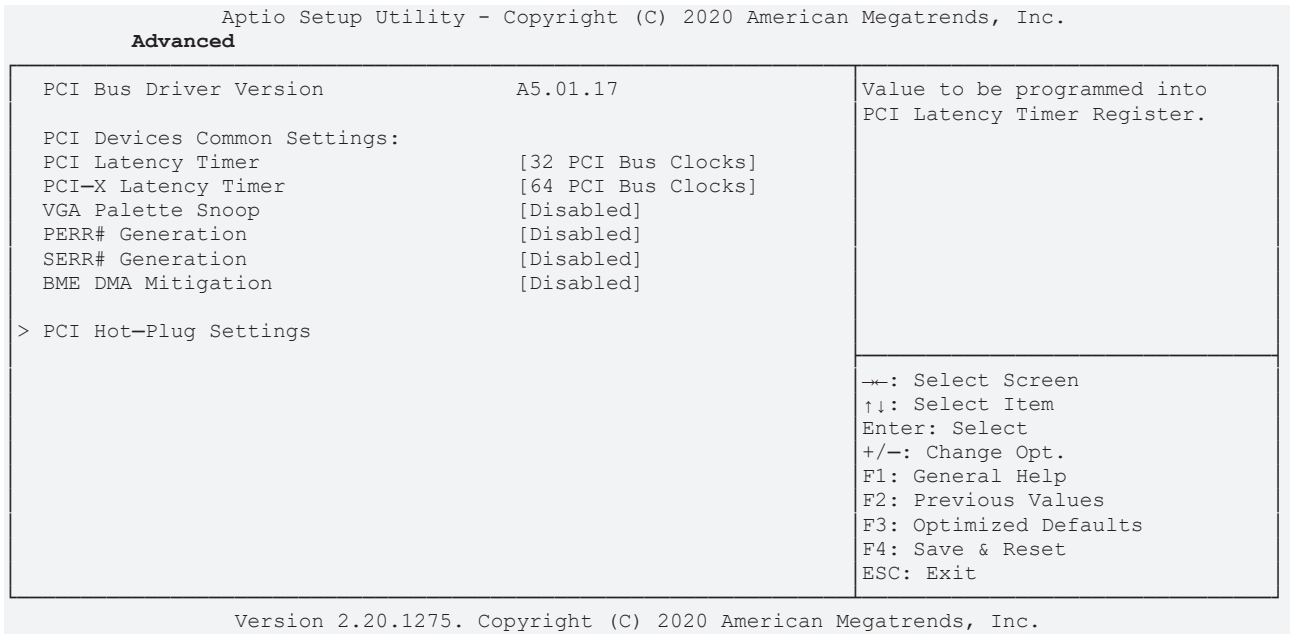
BIOS entry	Options
PC Health Status	
CPU dig.	None
PwrCtrlTemp	None
PwrCtrlVCC	None

8.3.8 AMI Graphic Output Protocol Policy



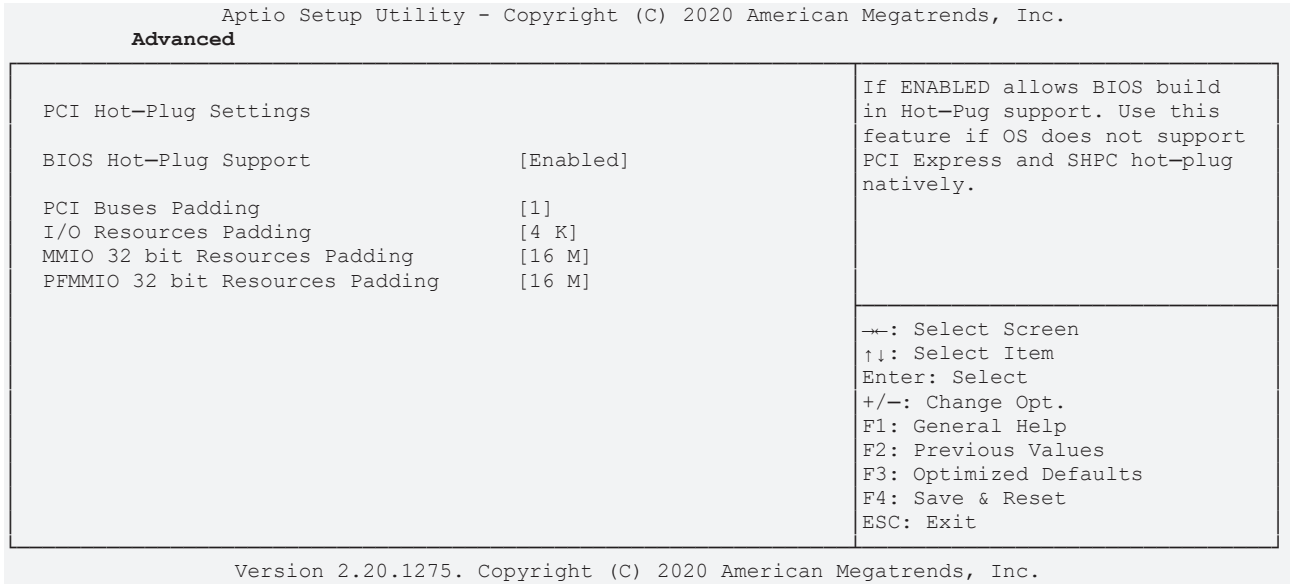
BIOS entry	Options
Intel® Graphics Controller Intel® GOP Driver [9.0.1105]	
Output select	DVI1

8.3.9 PCI Subsystem Settings



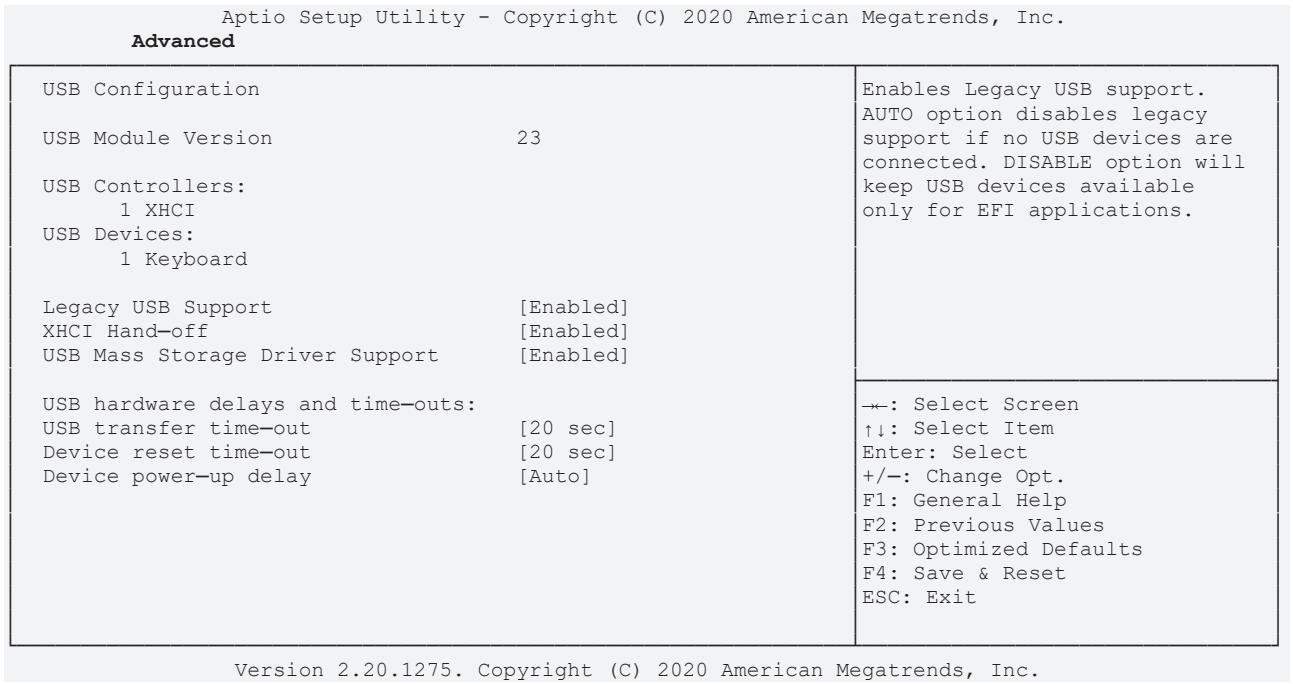
BIOS entry	Options
PCI bus driver version	None
PCI device common settings:	
PCI latency timer	32 / 64 / 96 / 128 / 160 /192 / 224 / 248 / PCI bus clock
PCI-X latency timer	32 / 64 / 96 / 128 / 160 /192 / 224 / 248 / PCI bus clock
VGA palette snoop	Disabled / Enabled
PERR# generation	Disabled / Enabled
SERR# generation	Disabled / Enabled
Above 4G Decoding	Disabled / Enabled
PCI Hot-Plug Settings	Submenu see: PCI Hot-Plug Settings [▶ 38]

8.3.9.1 PCI Hot-Plug Settings



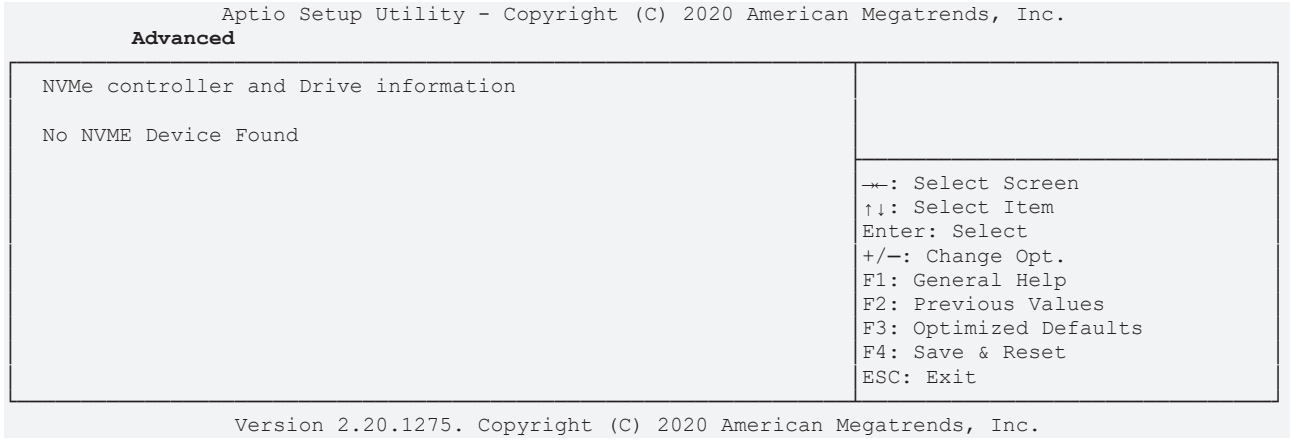
BIOS entry	Options
PCI Hot-Plug Settings	
BIOS hot-plug support	Enabled / Disabled
PCI buses padding	Disabled / 1 / 2 / 3 / 4 / 5
I/O resources padding	Disabled / 4 K / 8 K / 16 K / 32 K
MMIO 32 bit resources padding	Disabled / 1 M / 2 M / 4 M / 8 M / 16 M / 32 M / 64 M / 128 M
PFMMIO 32 bit resources padding	Disabled / 1 M / 2 M / 4 M / 8 M / 16 M / 32 M / 64 M / 128 M

8.3.10 USB Configuration



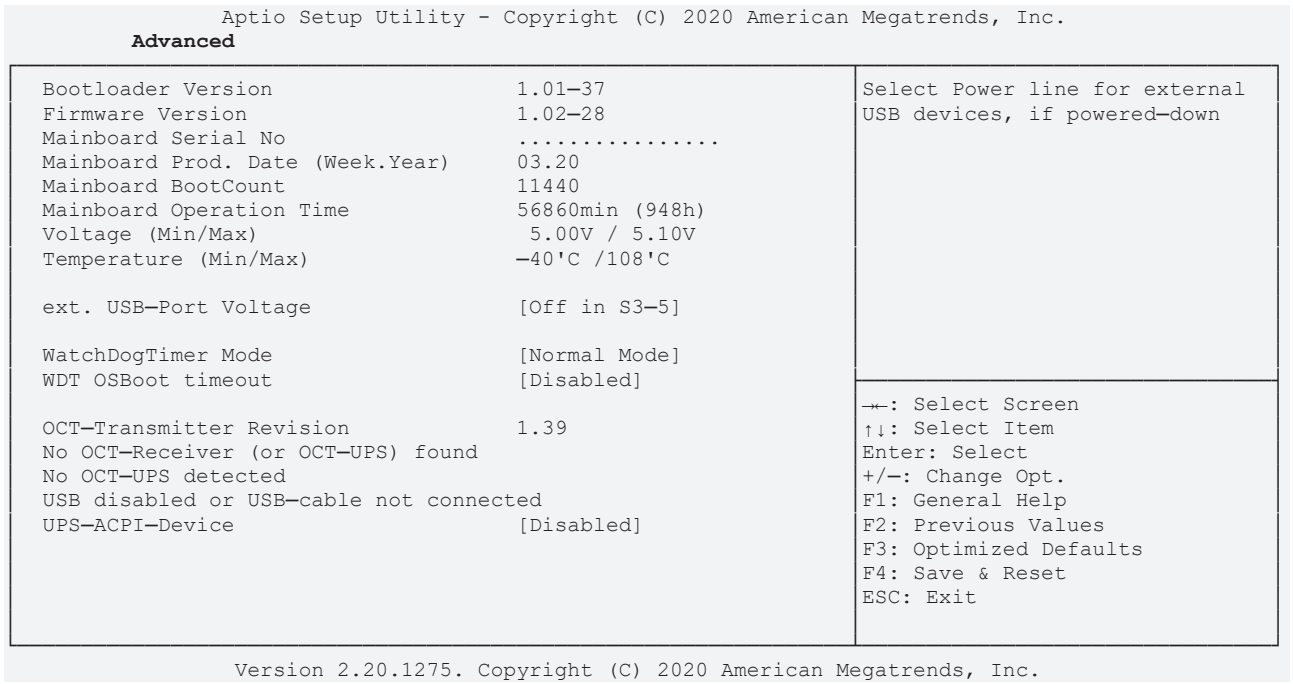
BIOS entry	Options
USB Configuration	
USB Module Version	None
USB Controllers: 1 XHCI	None
USB Devices: 1 keyboard	None
Legacy USB support	Enabled / Disabled / Auto
XHCI Hand-off	Enabled / Disabled
USB Mass Storage Driver Support	Enabled / Disabled
USB hardware delays and time-outs:	
USB transfer time-out	1 / 5 / 10 / 20 sec
Device reset time-out	10 / 20 / 30 / 40 sec
Device power-up delay	Auto / Manual

8.3.11 NVMe Configuration



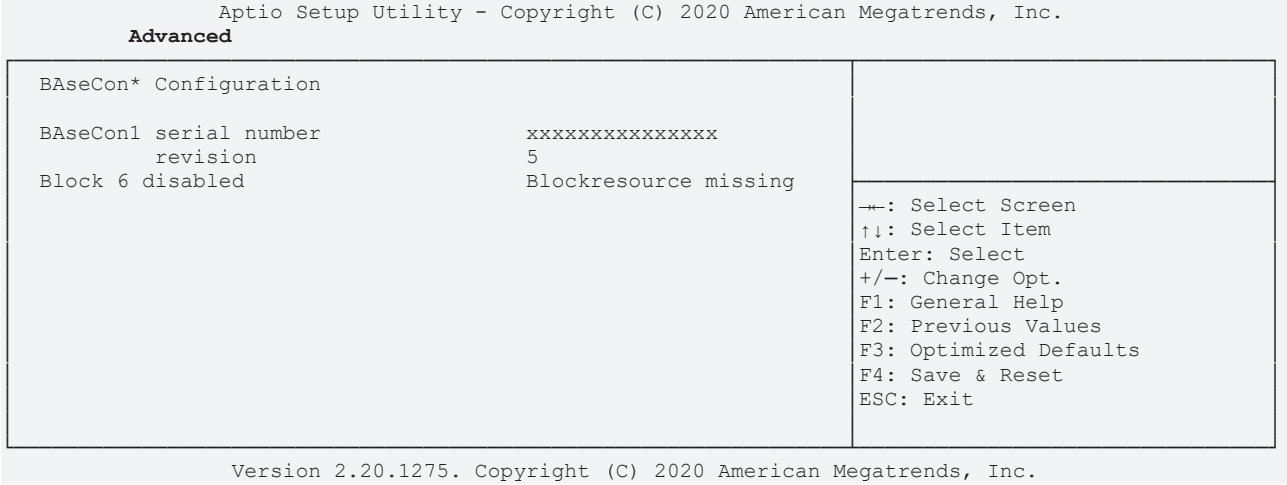
BIOS entry	Options
NVMe controller and drive information	
No NVME device found	None

8.3.12 Power Controller Options



BIOS entry	Options
Bootloader version	None
Firmware version	None
Mainboard serial no	None
Mainboard Prod. Date (Week.Year)	None
Mainboard BootCount	None
Mainboard operation time	None
Voltage /Min/Max)	None
Temperature (Min/Max)	None
ext. USB port voltage	Off in S3-5 / by SCVV
WatchDogTimer mode	Normal mode / Compatibility mode
WDT OSBoot Timeout	Disabled / 45 / 60 / ... / 255 seconds
OCT transmitter revision	None
No OCT receiver (or OCT_UPS) found	None
No OCT UPS detected	None
USB disabled or USB cable not connected	None
UPS ACPI device	Disabled / Prefer OCT / Prefer USB / Use OCT / Use USB

8.3.13 BAseCon* Configuration



BIOS entry	Options
BAseCon* Configuration	
BAseCon 1 serial number revision	None None
Block 6 disabled	None

*Old name for BeaCon140.

8.3.14 SATA And RST Configuration

```
                Aptio Setup Utility - Copyright (C) 2020 American Megatrends, Inc.
          Advanced
```

SATA And RST Configuration		Enable/Disable SATA Device.
SATA Controller(s)	[Enabled]	
SATA Mode Selection	[Intel RST Premium] With Intel Optane System Acceleration]	
SATA Interrupt Selection	[Msix]	
SATA Test Mode	[Disabled]	
RAID Device ID	[Client]	
> Software Feature Mask Configuration		
Aggressive LPM Support	[Disabled]	
Serial ATA Port 0	Empty	
Software Preserve	Unknown	
Port 0	[Enabled]	
Hot Plug	[Disabled]	
Configured as eSATA	Hot Plug supported	
External	[Disabled]	→←: Select Screen
Spin Up Device	[Disabled]	↑↓: Select Item
SATA Device Type	[Hard Disk Drive]	Enter: Select
SATA Port 0 DevSlp	[Disabled]	+/−: Change Opt.
DITO Configuration	[Disabled]	F1: General Help
Serial ATA Port 1	Empty	F2: Previous Values
Software Preserve	Unknown	F3: Optimized Defaults
Port 1	[Enabled]	F4: Save & Reset
Hot Plug	[Disabled]	ESC: Exit
Configured as eSATA	Hot Plug supported	
External	[Disabled]	
Spin Up Device	[Disabled]	
SATA Device Type	[Hard Disk Drive]	
SATA Port 1 DevSlp	[Disabled]	
DITO Configuration	[Disabled]	
Serial ATA Port 2	Empty	
Software Preserve	Unknown	
Port 2	[Enabled]	
Hot Plug	[Disabled]	
Configured as eSATA	Hot Plug supported	
External	[Disabled]	
Spin Up Device	[Disabled]	
SATA Device Type	[Hard Disk Drive]	
SATA Port 2 DevSlp	[Disabled]	
DITO Configuration	[Disabled]	

```
                Version 2.20.1275. Copyright (C) 2020 American Megatrends, Inc.
```

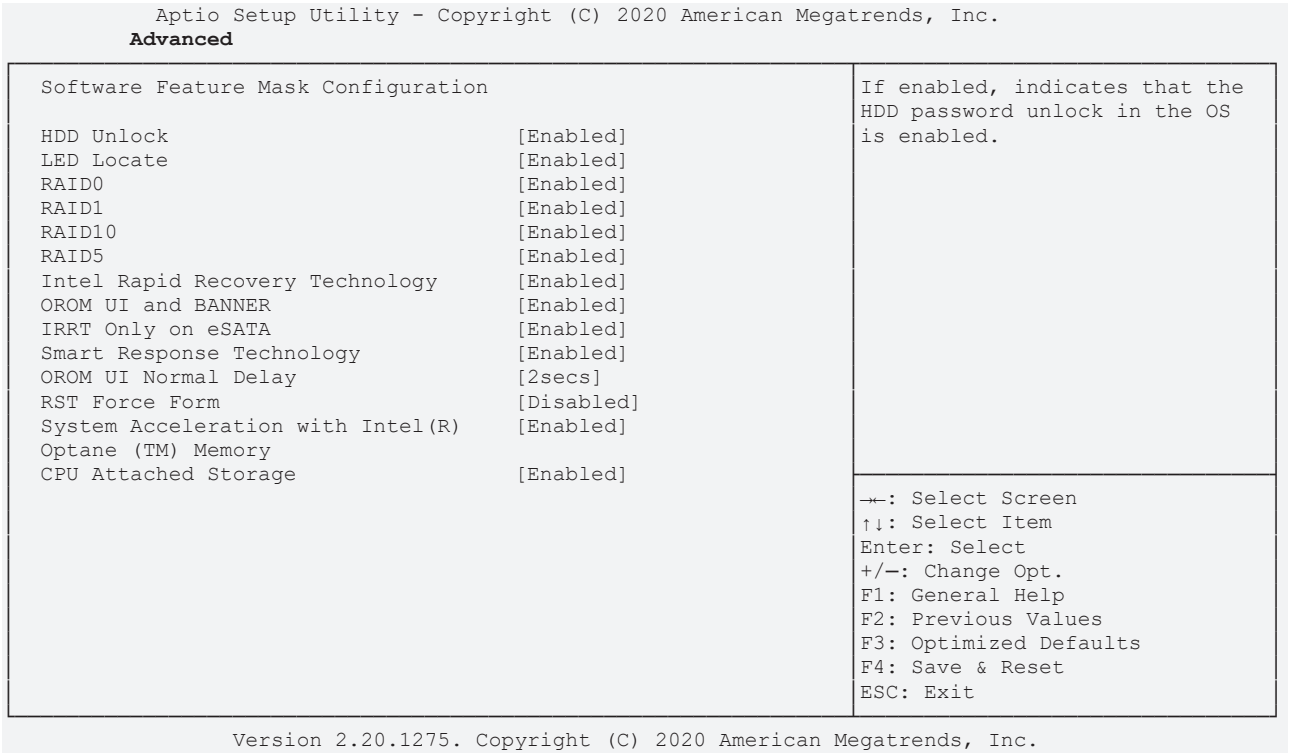
BIOS entry	Options
SATA And RST Configuration	
SATA controller(s)	Enabled / Disabled
SATA mode selection	AHCI / Intel RST Premium With Intel Optane System acceleration
SATA Test Mode	Disabled / Enabled
Software Feature Mask Configuration	Submenu see: Software Feature Mask Configuration [▶ 45]
Aggressive LPM support	Disabled / Enabled
Serial ATA port 0	None
Software Preserve	None
Port 0	Disabled / Enabled
Hot Plug	Disabled / Enabled
Configured as eSATA	None
External	Disabled / Enabled
spin-up device	Disabled / Enabled
SATA device type	HDD / SSD
SATA port 0 DevSlp	Disabled / Enabled
DITO configuration	Disabled / Enabled

NOTE

Serial ATA ports 0 - 2

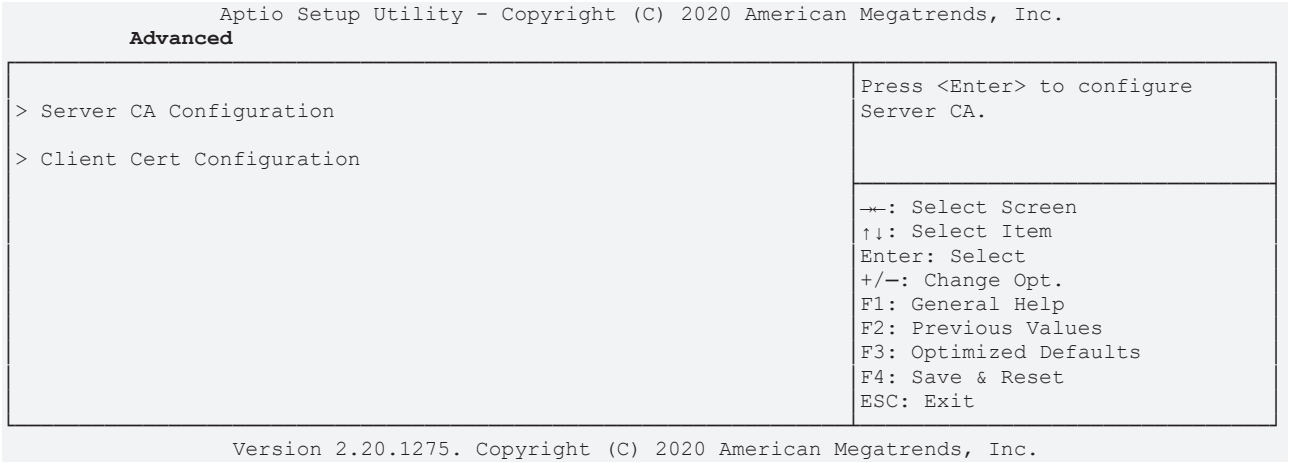
The identical BIOS entries for ports 0 – 2 are listed as examples for port 0.

8.3.14.1 Software Feature Mask Configuration



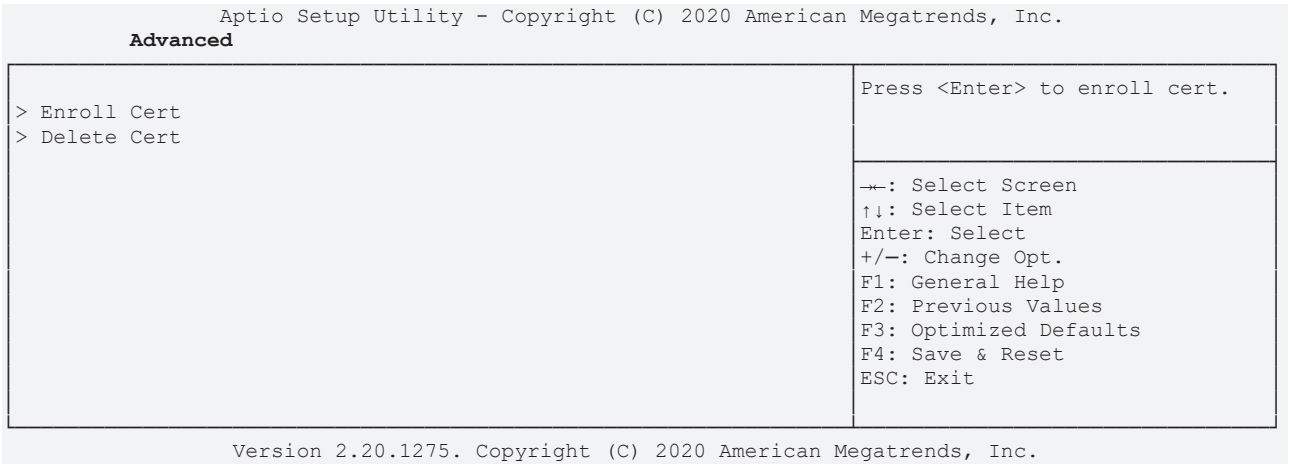
BIOS entry	Options
Software Feature Mask Configuration	
HDD Unlock	Enabled / Disabled
LED Locate	Enabled / Disabled
RAID0	Enabled / Disabled
RAID1	Enabled / Disabled
RAID10	Enabled / Disabled
RAID5	Enabled / Disabled
Intel Rapid Recovery Technology	Enabled / Disabled
OROM UI and BANNER	Enabled / Disabled
IRRT only on eSATA	Enabled / Disabled
Smart Response Technology	Enabled / Disabled
OROM UI normal delay	2 / 4 / 6 / 8 secs
RST Force Form	Disabled / Enabled
System acceleration with Intel® Optane™ memory	Enabled / Disabled
CPU attached storage	Enabled / Disabled

8.3.15 TLS Auth configuration



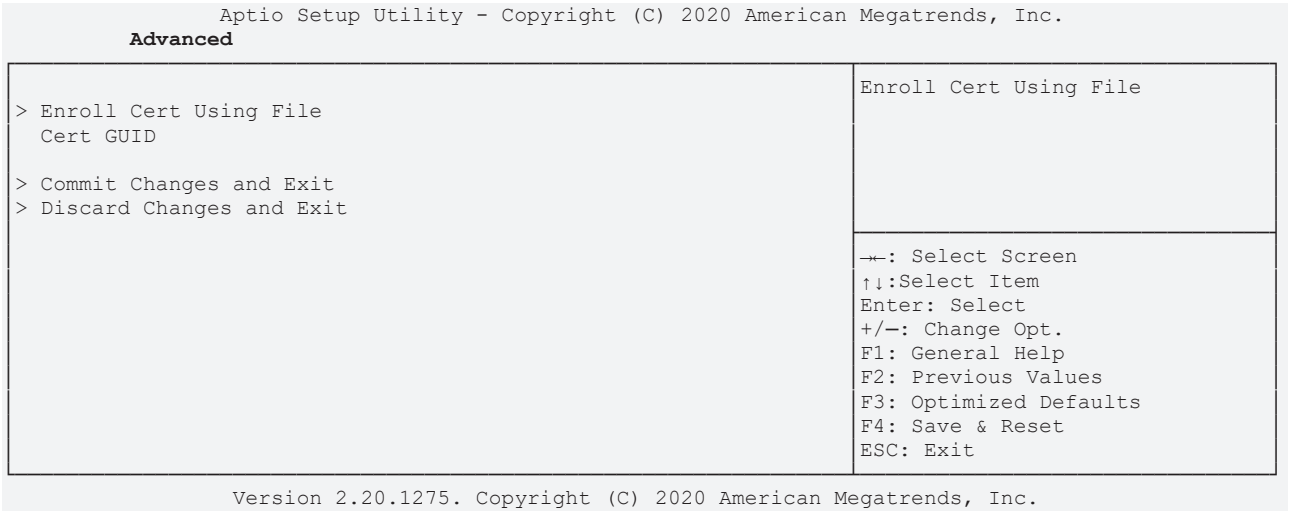
BIOS entry	Options
Server CA configuration	Submenu see: Server CA configuration [▶ 46]
Client cert configuration	None

8.3.15.1 Server CA configuration



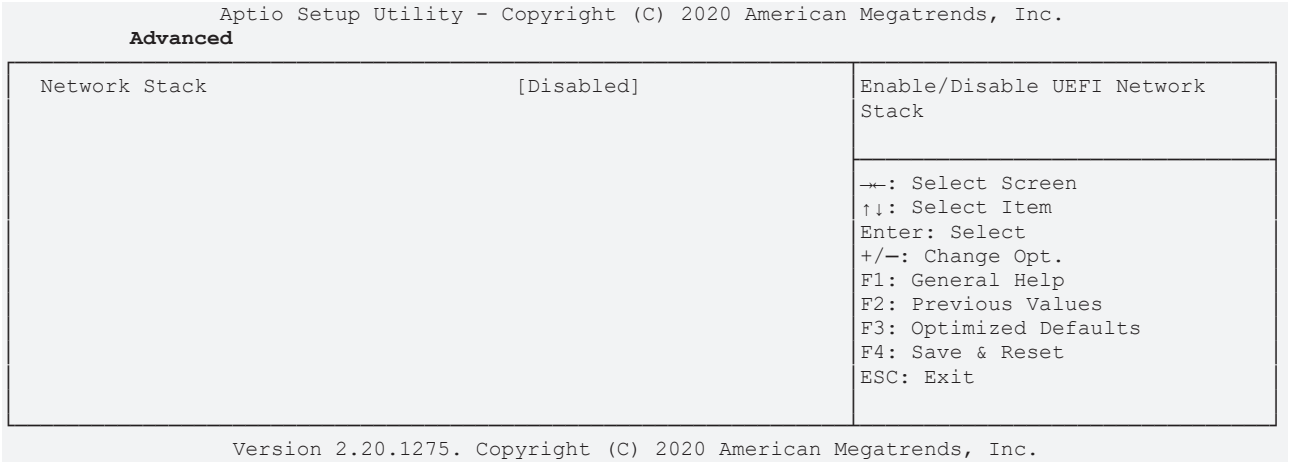
BIOS entry	Options
Enroll cert	Submenu see: Enroll cert
Delete cert	None

8.3.15.1.1 Enroll cert



BIOS entry	Options
Enroll cert using file	None
Cert GUID	None
Commit changes and exit	None
Discard changes and exit	None

8.3.16 Network Stack Configuration



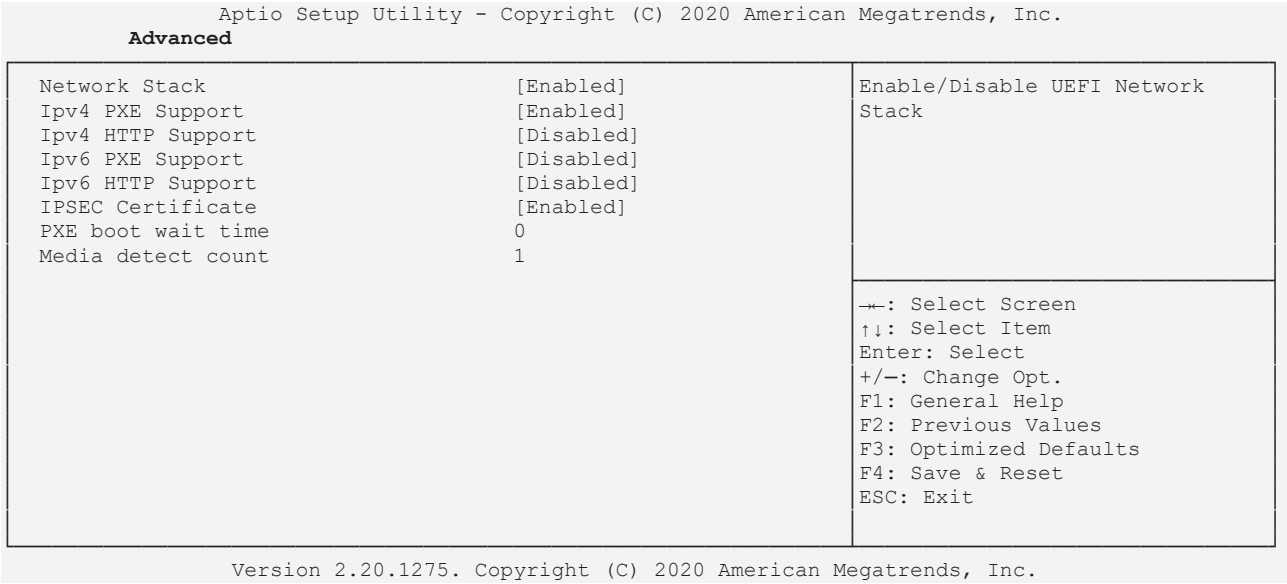
BIOS entry	Options
Network Stack	Disabled / Enabled

NOTE

Network stack enabled

If network stack is enabled, additional menu items for displaying and setting the LAN controllers are shown here. To do this, carry out a reset.

8.3.17 Network stack configuration enabled



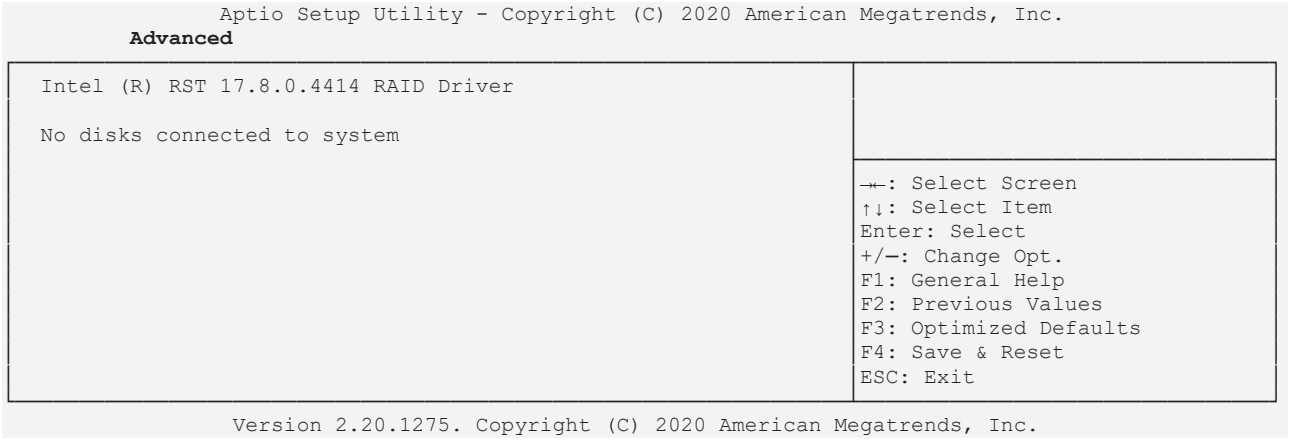
BIOS entry	Options
Network Stack	Disabled / Enabled
Ipv4 PXE Support	Disabled / Enabled
Ipv4 HTTP support	Disabled / Enabled
Ipv6 PXE Support	Disabled / Enabled
Ipv6 HTTP support	Disabled / Enabled
IPSEC certificate	Enabled / Disabled
PXE boot wait time	None
Media detect count	None

NOTE

PXE boot available

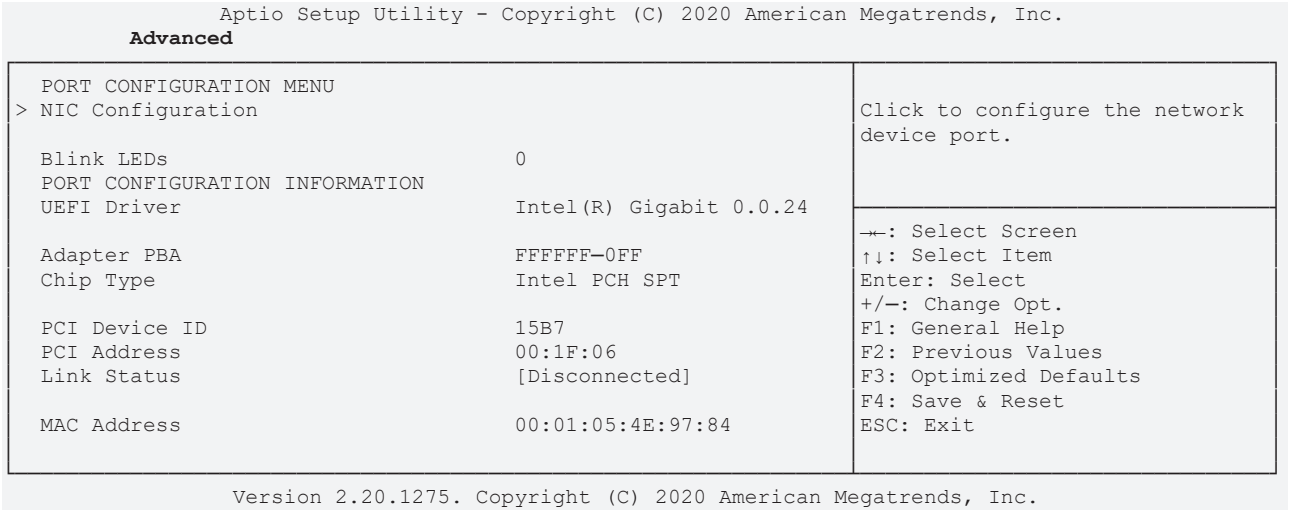
PXE boot is available if you set network stack and Ipv4 PXE support to "Enable".

8.3.18 Intel Rapid Storage Technology



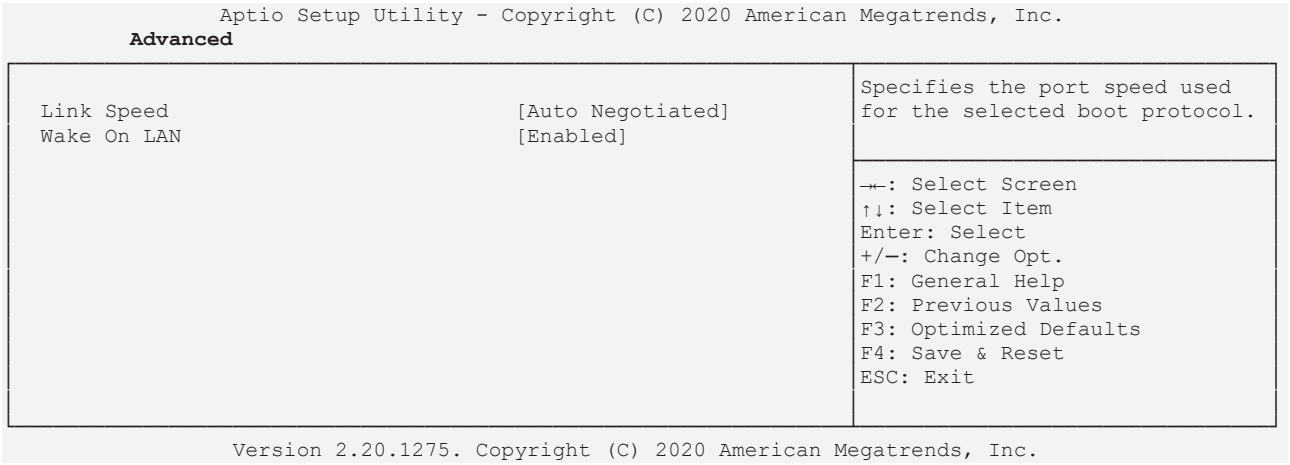
BIOS entry	Options
Intel® RST 17.8.0.4414 RAID driver	
No disks connected to system	None

8.3.19 Intel Ethernet connection(2) I219-LM



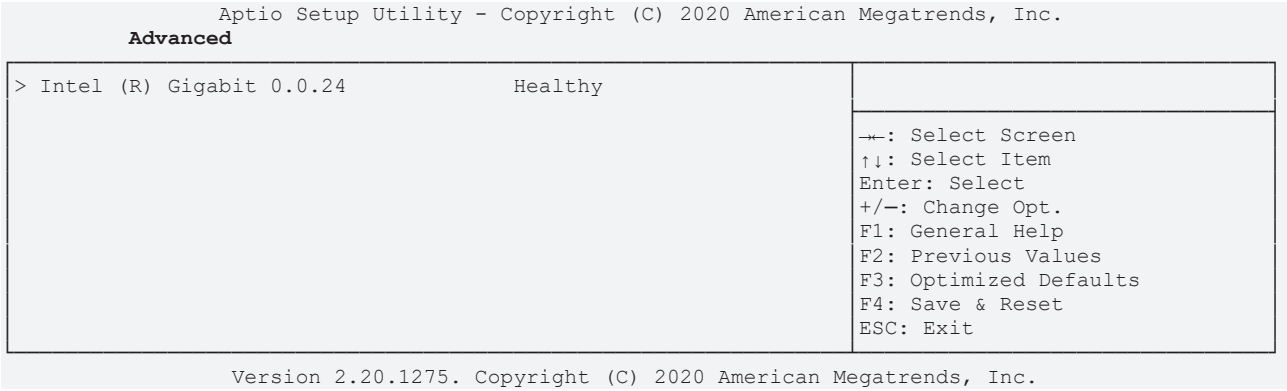
Bios entry	Options
PORT CONFIGURATION MENU	
NIC Configuration	See submenu: NIC Configuration [▶ 50]
Flashing LEDs	None
PORT CONFIGURATION INFORMATION	
UEFI driver	None
PBA adapter	None
Chip type	None
PCI device ID	None
PCI address	None
Link status	None
MAC Address	None

8.3.19.1 NIC Configuration



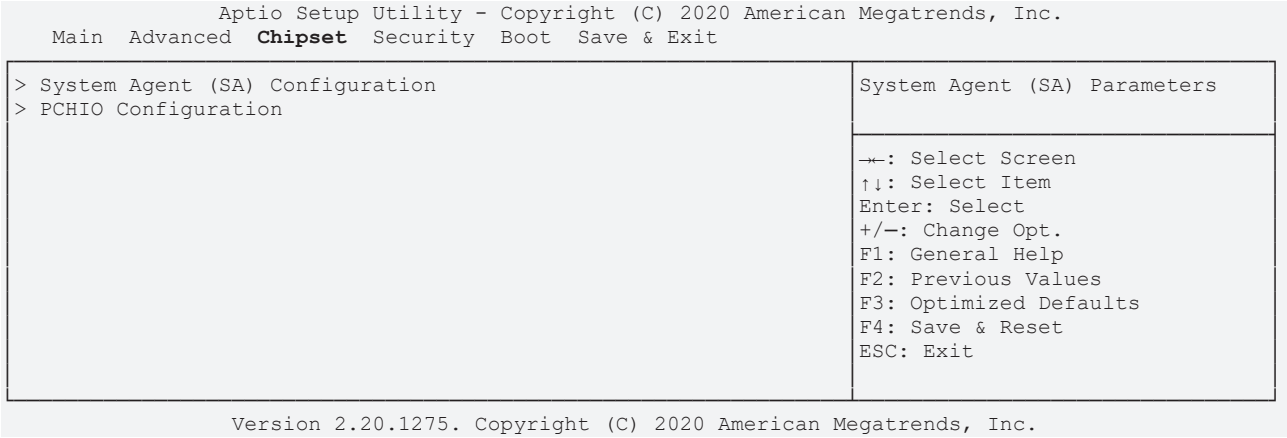
Bios entry	Options
Link speed	Auto Negotiated / 10 Mbps Half / 10 Mbps Full / 100 Mbps Half / 100 Mbps Full
Wake On LAN	Enabled / Disabled

8.3.20 Driver Health



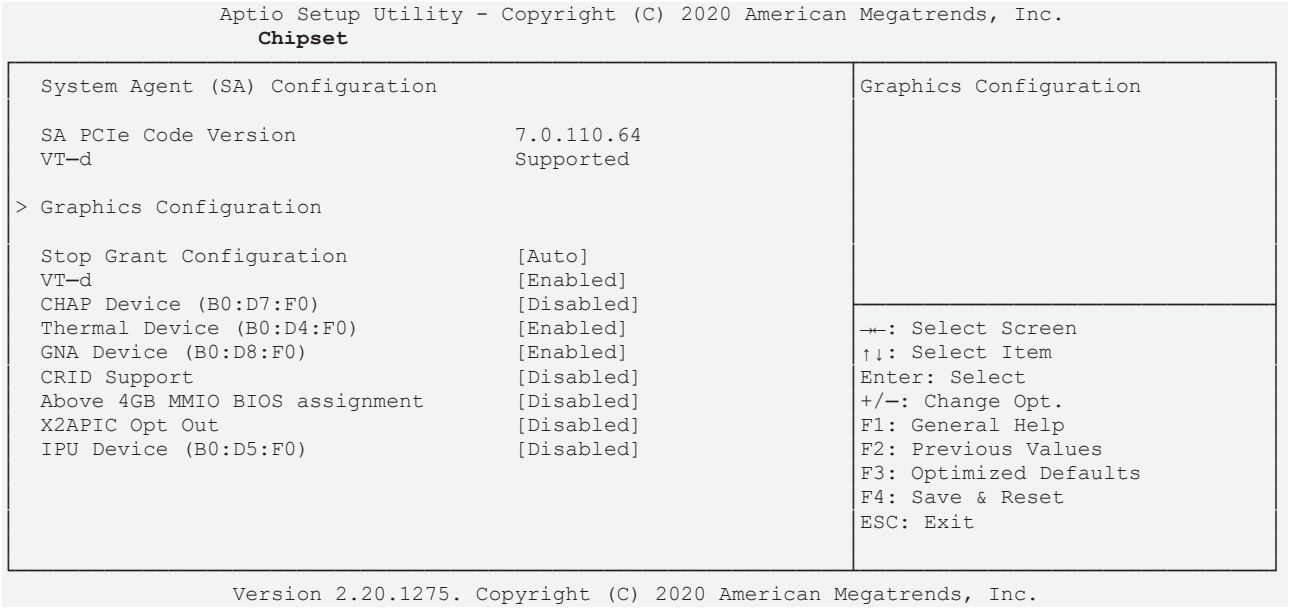
BIOS entry	Options
Intel® Gigabit 0.0.24	None

8.4 Chipset



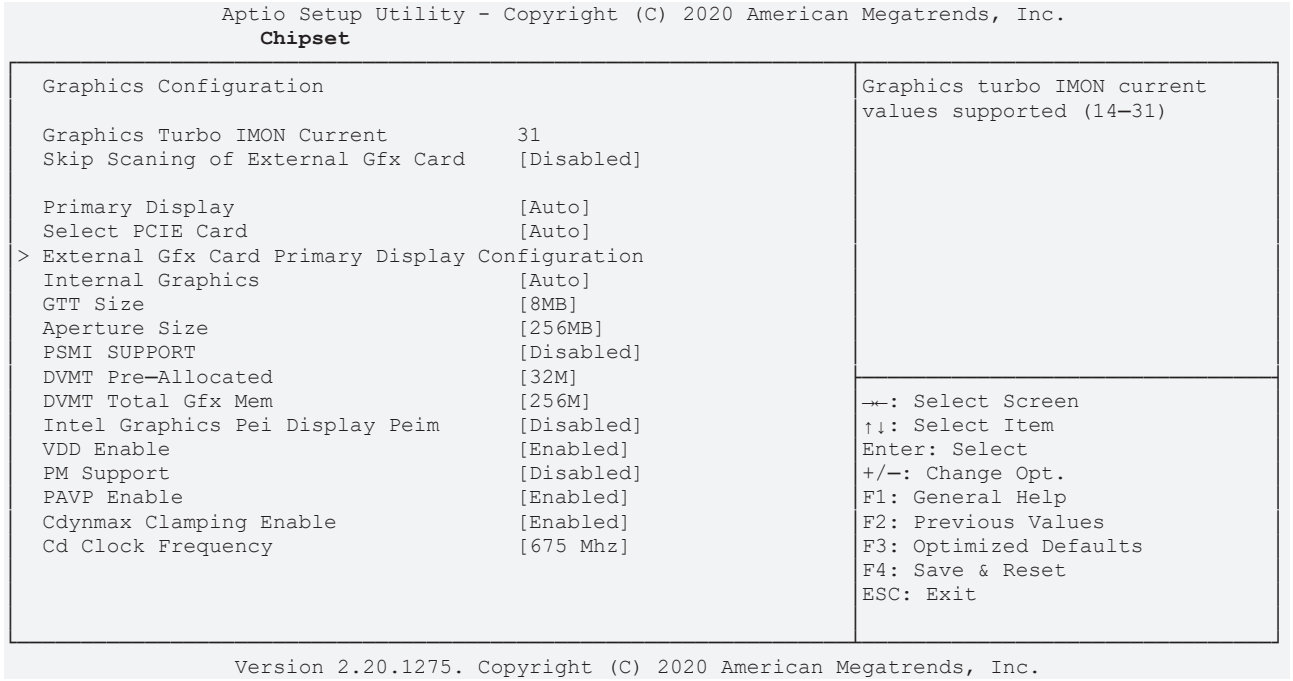
BIOS entry	Options
System Agent (SA) Configuration	Submenu see: System Agent SA Configuration [▶ 52]
PCH-IO Configuration	Submenu see: PCH-IO Configuration [▶ 54]

8.4.1 System Agent SA Configuration



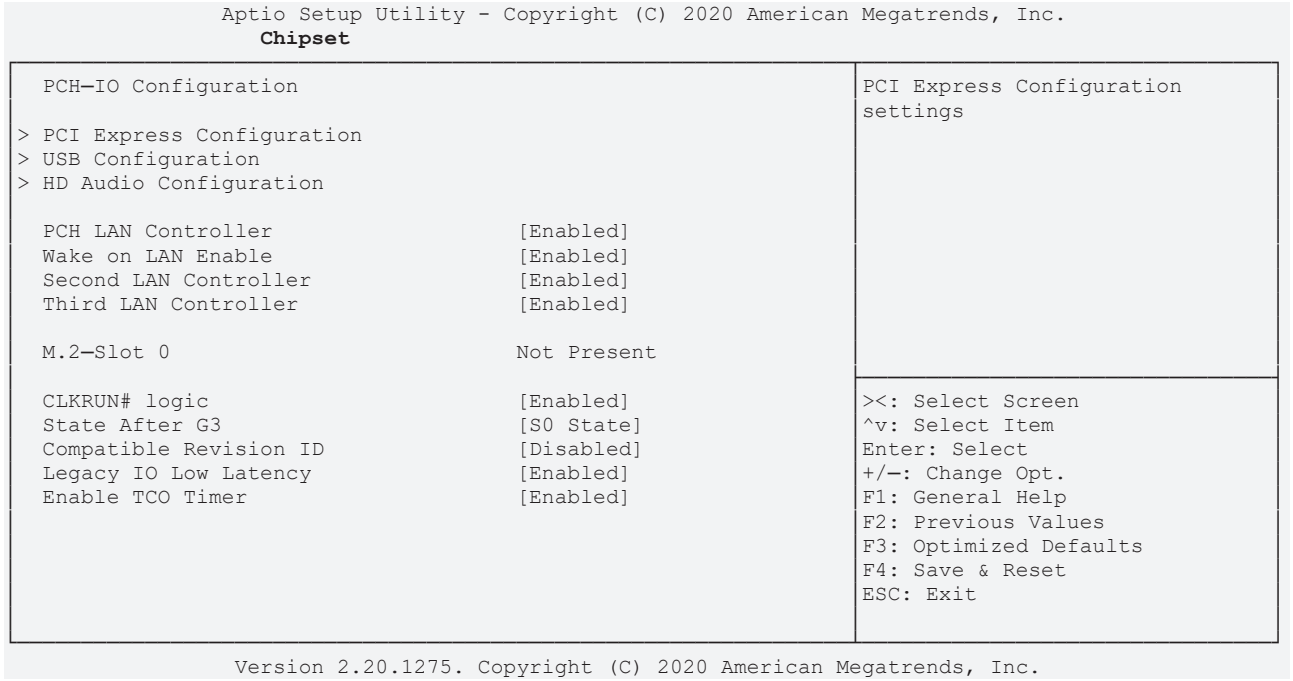
BIOS entry	Options
System Agent (SA) Configuration	
SA PCIe code version	None
VT-d	None
Graphics Configuration	Submenu see: Graphics Configuration [▶ 53]
Stop grant configuration	Auto / Manual
VT-d	Enabled / Disabled
CHAP device (B0:07:F0)	Disabled / Enabled
Thermal device (B0:D4:F0)	Enabled / Disabled
GNA device (B0:D8:F0)	Enabled / Disabled
CRID support	Disabled / Enabled
Above 4GB MMIO BIOS assignment	Disabled / Enabled
X2APIC Opt Out	Disabled / Enabled
IPU device (B0:D5:F0)	Disabled / Enabled

8.4.2 Graphics Configuration



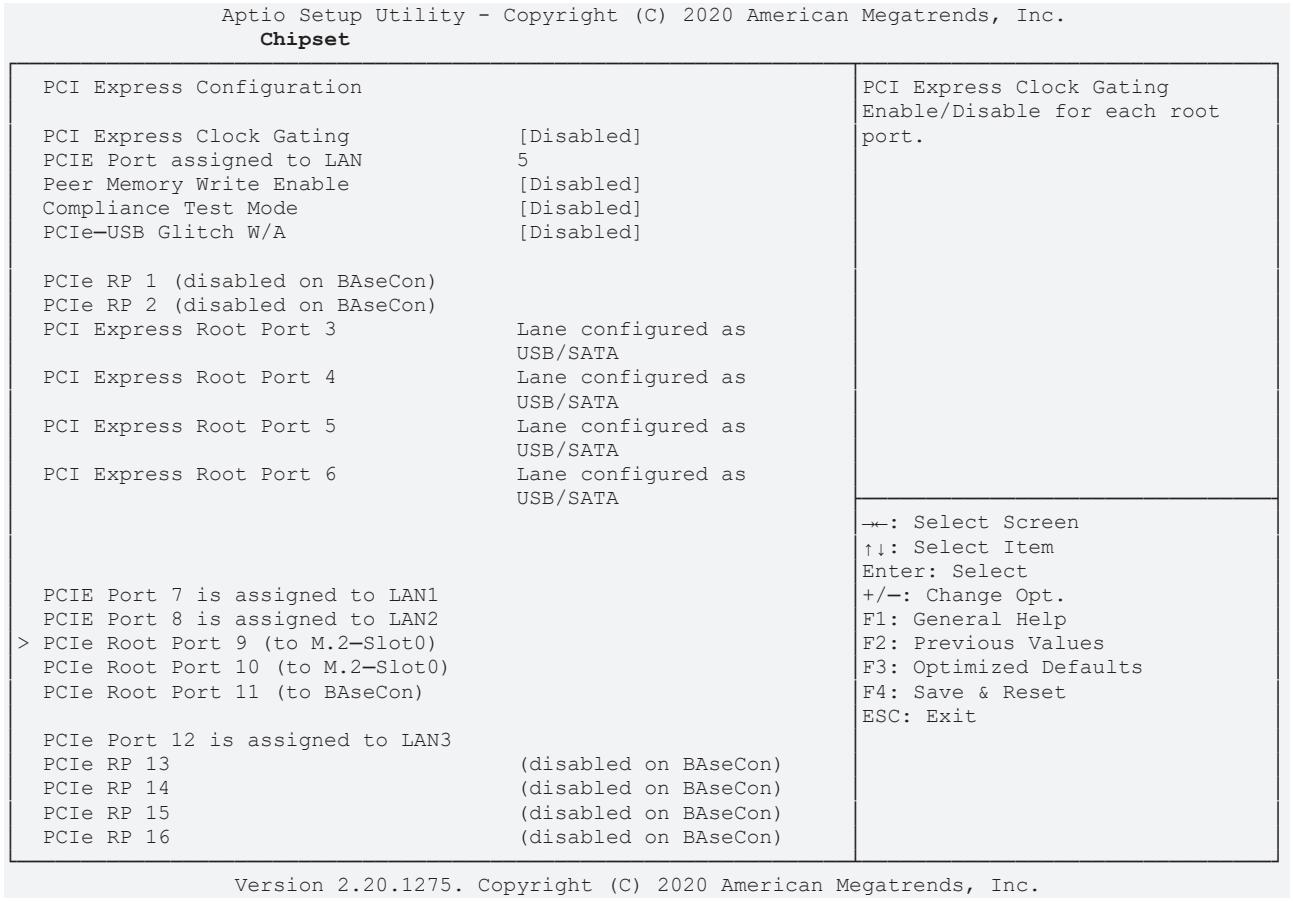
BIOS entry	Options
Graphics Configuration	
Graphics turbo IMON current	None
Skip Scanning of External Gfx Card	Disabled / Enabled
Primary Display	Auto / IGFX / PCI / SG
Select PCIE Card	Auto / Elk Creek 4 / PEG Eval
External Gfx Card Primary Display Configuration	None
Internal Graphics	Auto / Disabled / Enabled
GTT Size	2 / 4 / 8 MB
Aperture Size	128 / 256 / 512 / 1024 / 2048 MB
PSMI SUPPORT	Disabled / Enabled
DVMT Pre-Allocated	0M / 32M…60M
DVMT Total Gfx Mem	128M / 256M / MAX
Intel Graphics Pei Display Peim	Disabled / Enabled
VDD Enable	Enabled / Disabled
PM support	Disabled / Enabled
PAVP Enable	Enabled / Disabled
Cdynmax Clamping Enable	Enabled / Disabled
Cd Clock Frequency	337.5 / 450 / 540 / 675 Mhz

8.4.3 PCH-IO Configuration



BIOS entry	Options
PCH-IO Configuration	
PCI Express Configuration	Submenu see: PCI express configuration (Q370) [▶ 55]
USB Configuration	Submenu see: USB Configuration [▶ 59]
HD Audio Configuration	Submenu see: HD Audio Configuration [▶ 59]
PCH LAN controller	Enabled / Disabled
Wake on LAN Enable	Enabled / Disabled
Second LAN controller	Enabled / Disabled
Third LAN controller	Enabled / Disabled
M.2 slot 0	None
CLKRUN# logic	Enabled / Disabled
State after G3	S0 state / S5 state
Compatible revision ID	None
Legacy IO low latency	Enabled / Disabled
Enable TCO timer	Enabled / Disabled

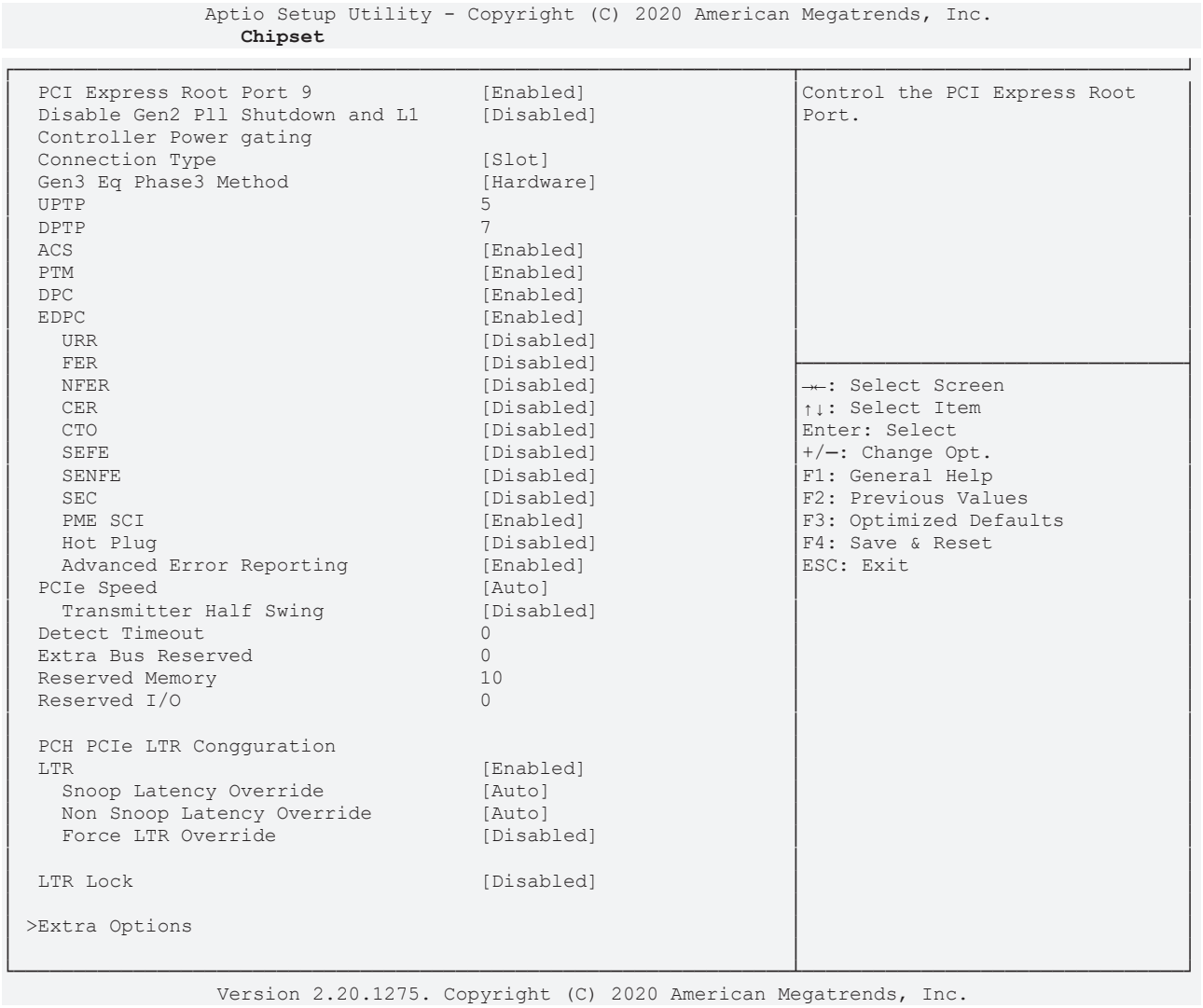
8.4.3.1 PCI express configuration (Q370)



BIOS entry	Options
PCI Express Configuration	
PCI express clock gating	Disabled / Enabled
PCIE port assigned to LAN	None
Peer memory write enable	Disabled / Enabled
Compliance test mode	Disabled / Enabled
PCIe USB glitch W/A	Disabled / Enabled
PCIe RP 1 (disabled on BAseCon)	Disabled / Enabled
PCIe RP 2 (disabled on BAseCon)	Disabled / Enabled
PCI express root port 3	None
PCI express root port 4	None
PCI express root port 5	None
PCI express root port 6	None
PCIe root port 7 is assigned to LAN1	None
PCIe root port 8 is assigned to LAN2	None
PCIe root port 9 (to M.2 slot0)	Enabled / Disabled
PCIe root port 10 (to M.2 slot0)	Enabled / Disabled
PCIe root port 11 (to BAseCon)	Enabled / Disabled
PCIe port 12 is assigned to LAN3	None
PCIe RP 13 (disabled on BAseCon)	Disabled / Enabled
PCIe RP14 (disabled on BAseCon)	Disabled / Enabled
PCIe RP 15 (disabled on BAseCon)	Disabled / Enabled
PCIe RP 16 (disabled on BAseCon)	Disabled / Enabled

*Old name for BeaCon140.

8.4.3.1.1 PCI express root port 9



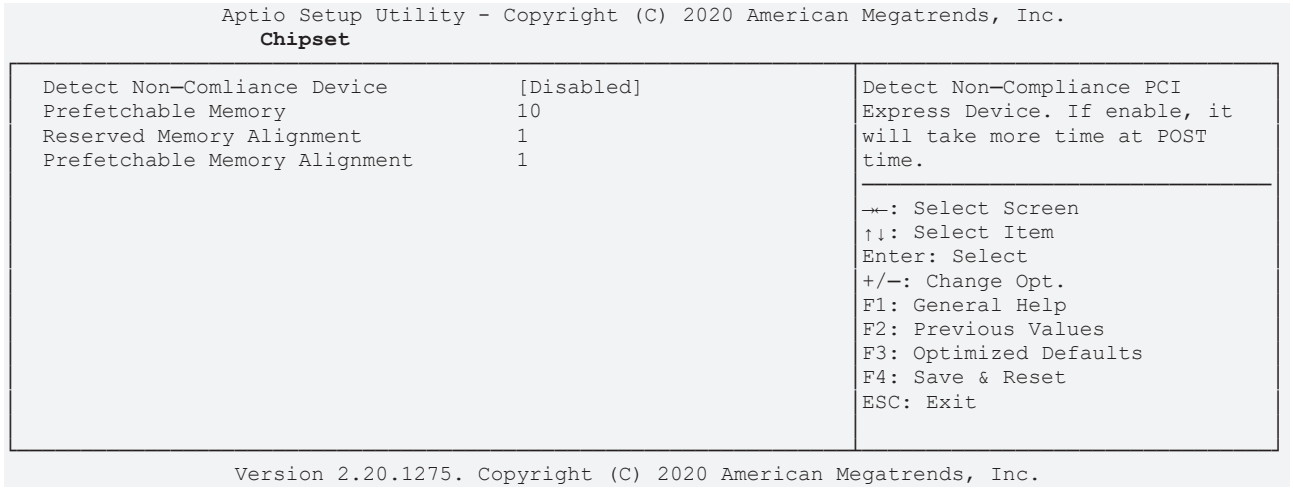
BIOS entry	Options
PCI express root port 9	Disabled / Enabled

NOTE

PCI Express Configuration

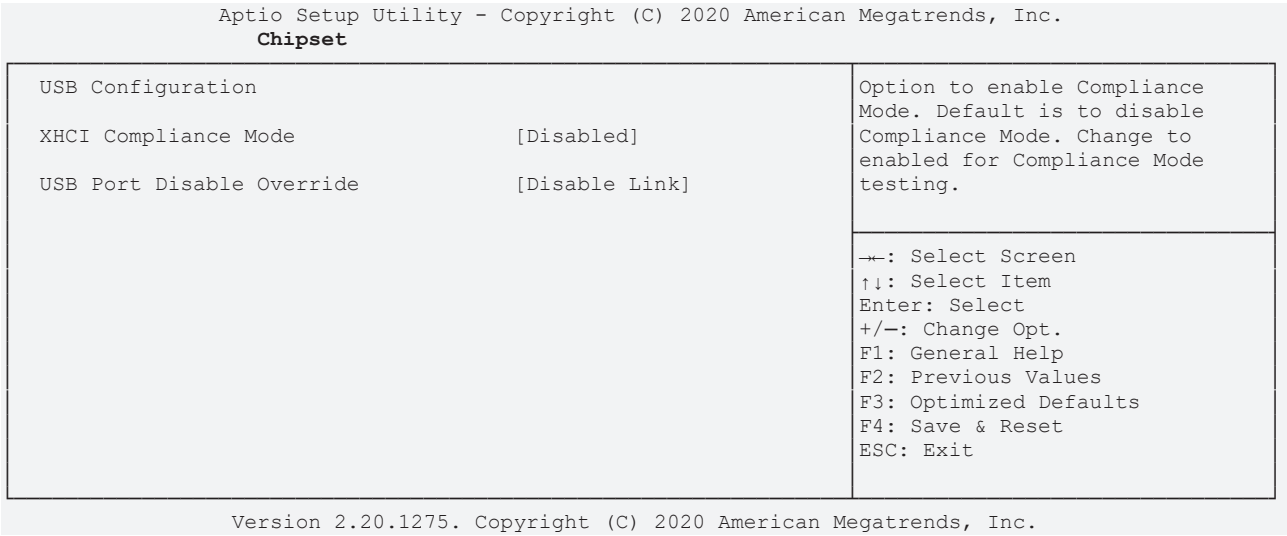
The BIOS entries are shown here for port 9 as an example. For activation set the PCI Express root ports to “Enabled”.

Extra Options



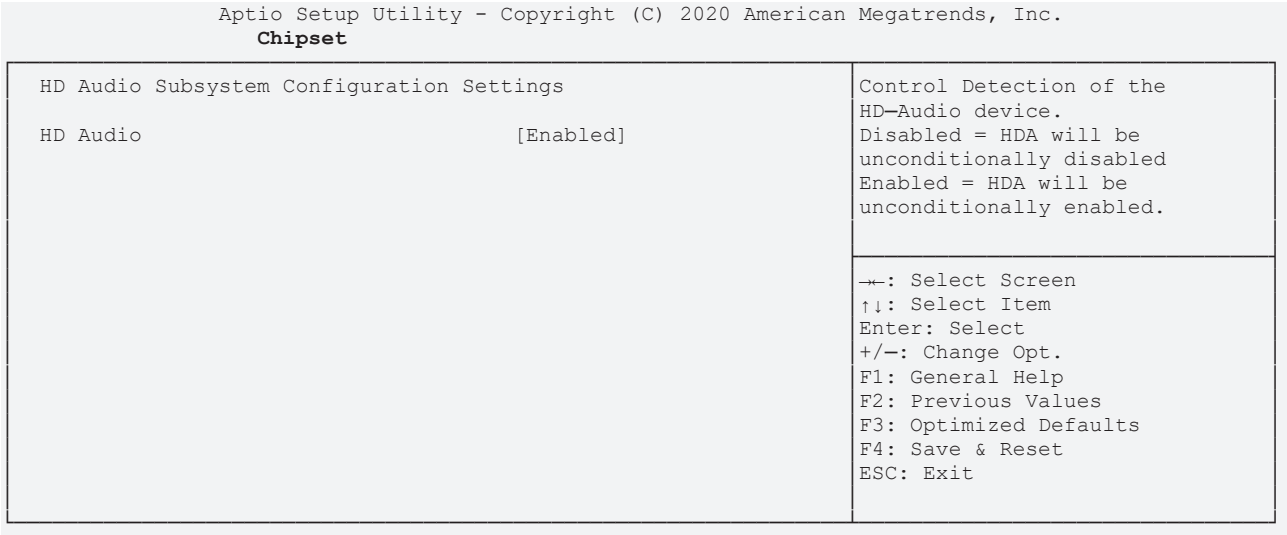
BIOS entry	Options
Detect non-compliance device	Disabled / Enabled
Prefetchable Memory	None
Reserved Memory Alignment	None
Prefetchable Memory Alignment	None

8.4.3.2 USB Configuration



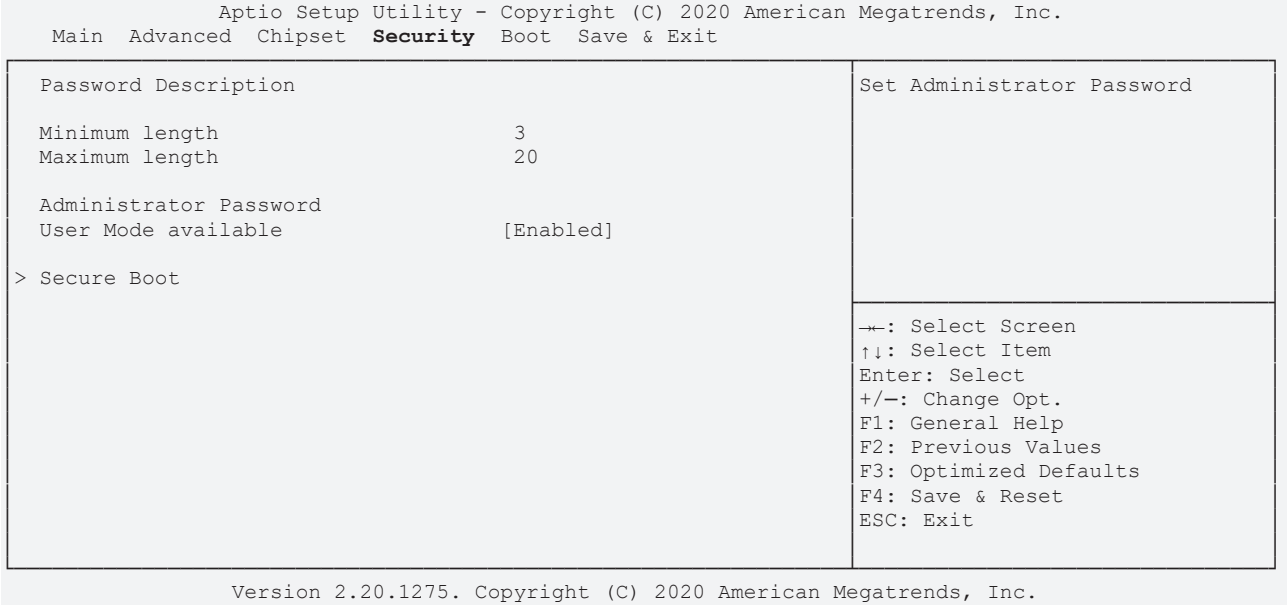
BIOS entry	Options
USB Configuration	
XHCI compliance mode	Disabled / Enabled
USB port disable override	Disable link / Select per-pin

8.4.3.3 HD Audio Configuration



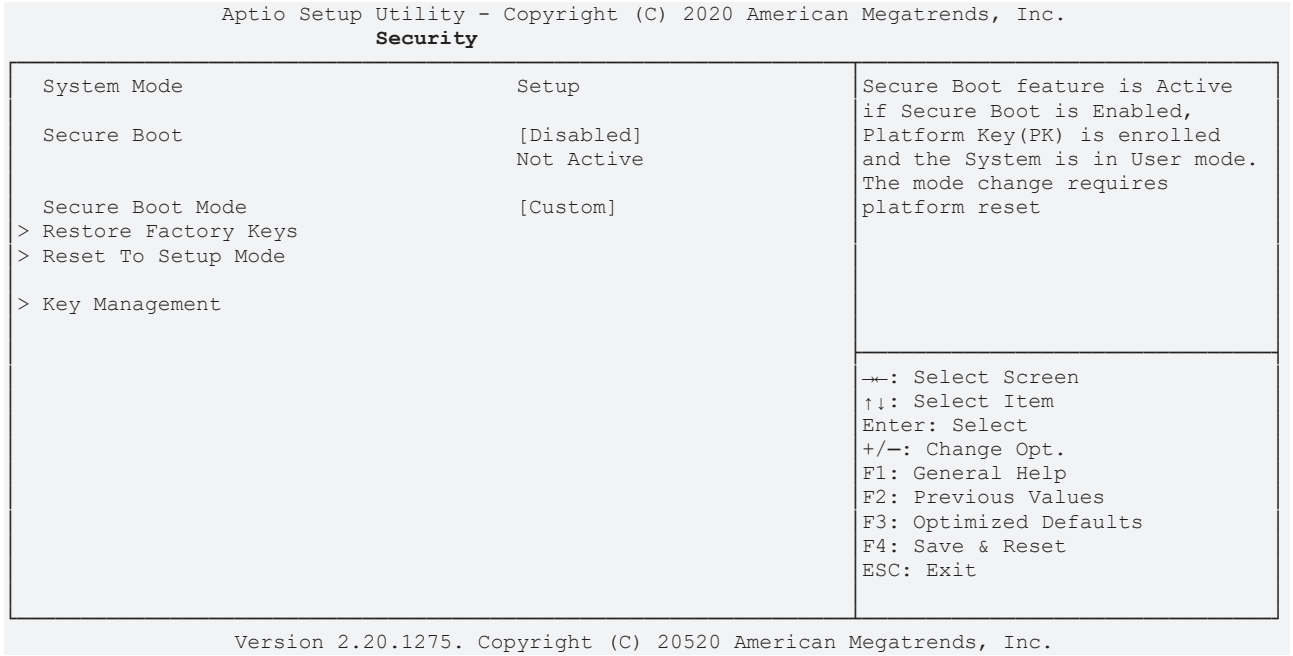
BIOS entry	Options
HD audio subsystem configuration settings	
HD audio	Enabled / Disabled

8.5 Security



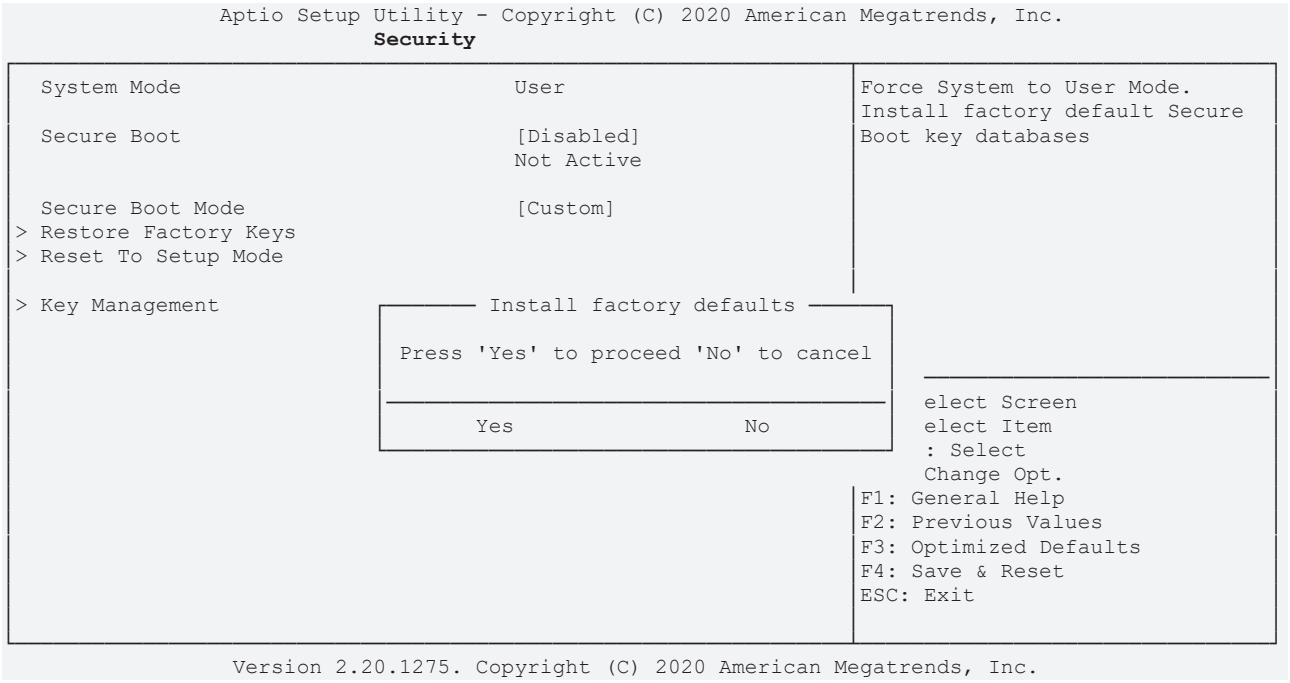
BIOS entry	Options
Password Description	
Minimum Length	None
Maximum Length	None
Administrator Password	Here you can set an administrator password.
User mode available	Enabled / Disabled
Secure Boot menu	Submenu see: Secure Boot [▶ 61]

8.5.1 Secure Boot



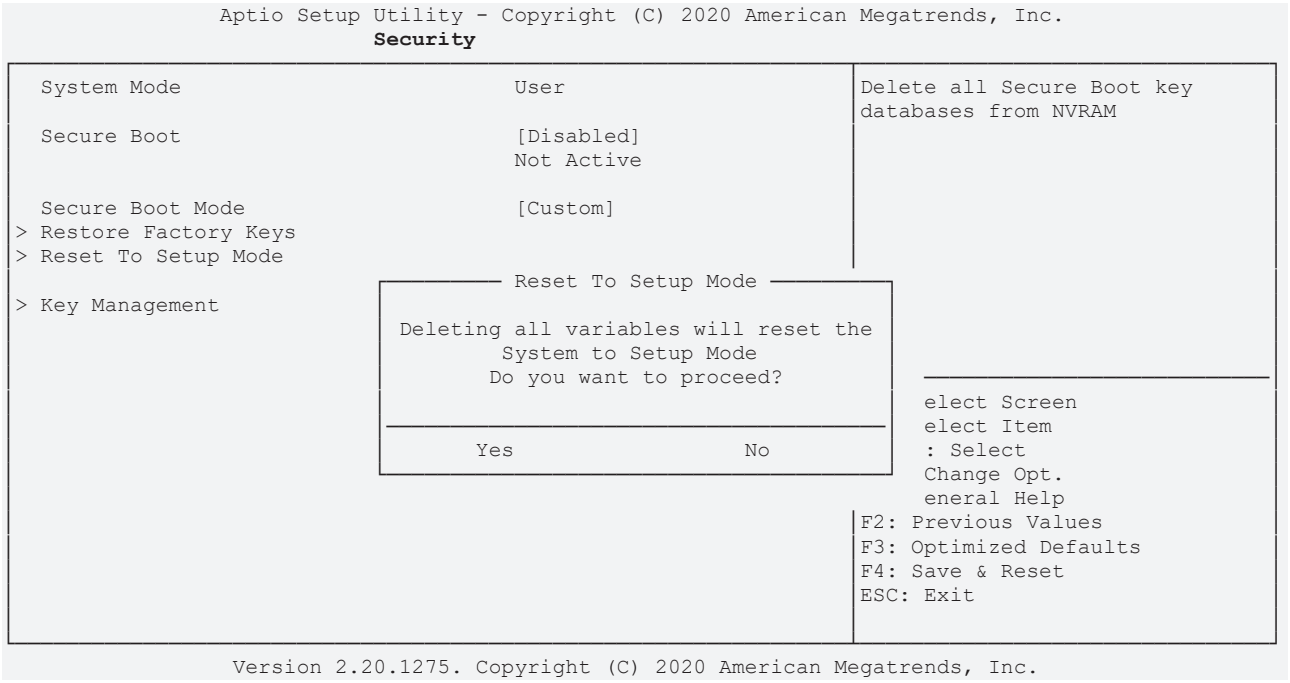
Bios entry	Options
System Mode	None
Secure Boot	Disabled / Enabled Not Active
Secure Boot Mode	Custom / Standard
Restore factory keys	Submenu see: Restore factory keys [▶ 62]
Reset To Setup Mode	Submenu see: Reset To Setup Mode [▶ 63]
Key Management	Submenu see: Key Management [▶ 64]

8.5.1.1 Restore factory keys



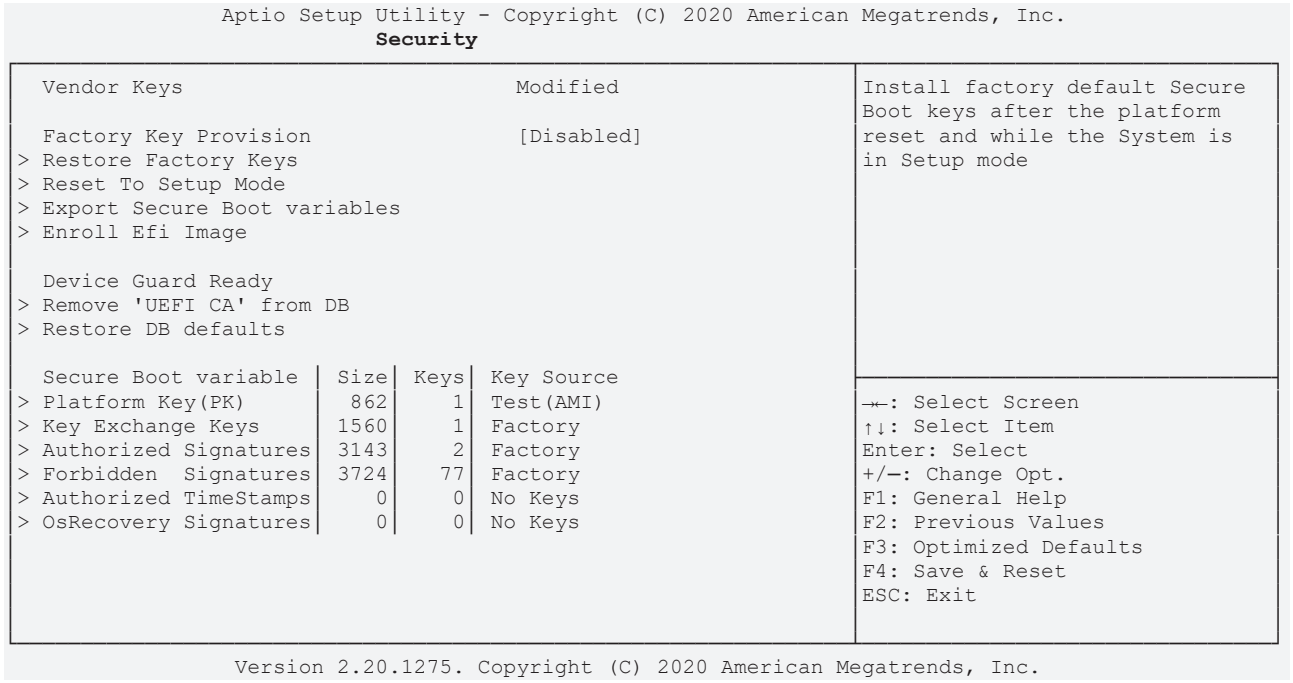
BIOS entry	Options
System Mode	None
Secure Boot	Disabled / Enabled Not Active
Secure Boot Mode	Custom / Standard
Restore factory keys	Install factory defaults (see box)

8.5.1.2 Reset To Setup Mode



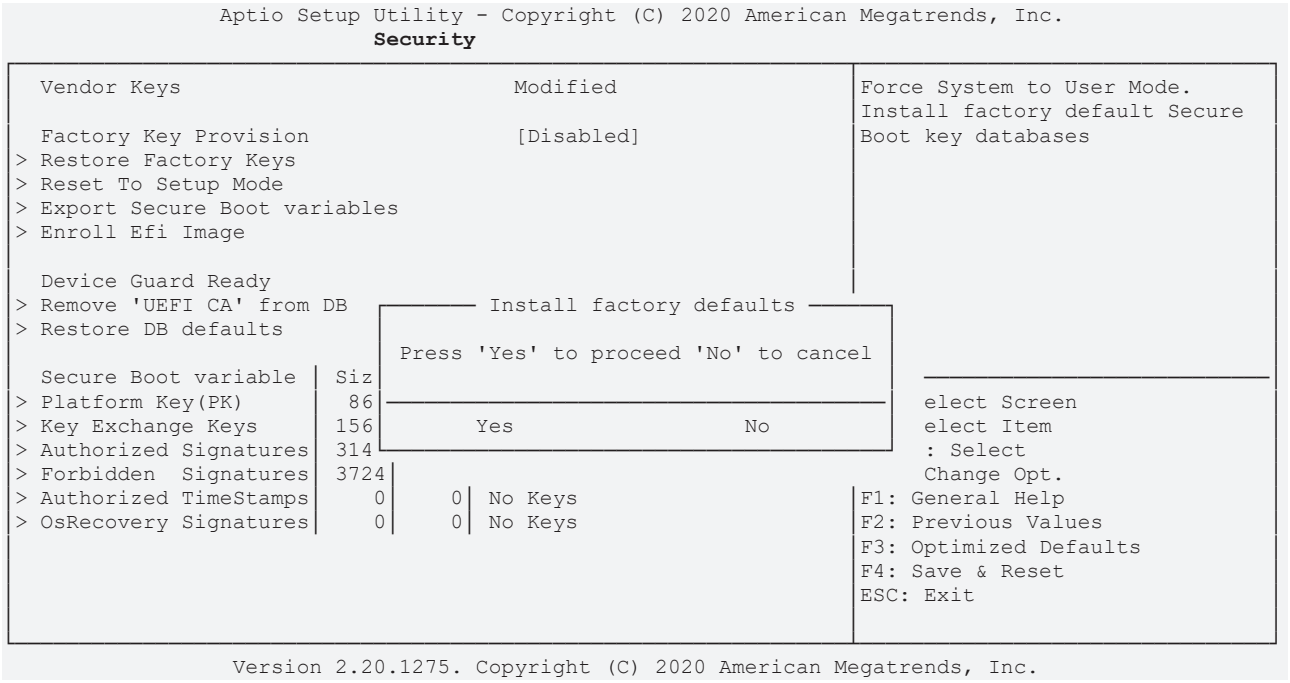
BIOS entry	Options
System Mode	none
Secure Boot	Disabled / Enabled Not Active
Secure Boot Mode	Custom / Standard
Reset To Setup Mode	Reset To Setup Mode (see box)

8.5.1.3 Key Management



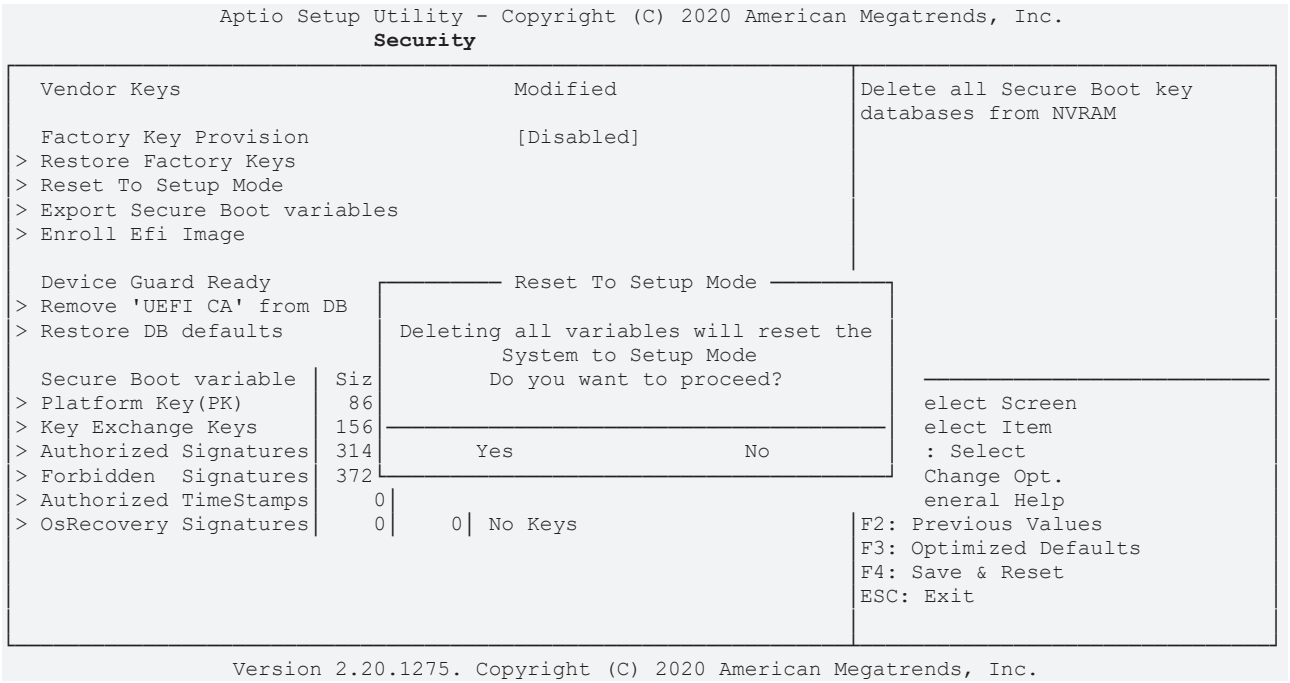
BIOS entry	Options
Vendor Keys	None
Factory key provision	Disabled / Enabled
Restore factory keys	Submenu see: Restore factory keys [▶ 65]
Reset To Setup Mode	Submenu see: Reset To Setup Mode [▶ 65]
Export Secure Boot variables	Submenu see: Export Secure Boot Variables [▶ 66]
Enroll Efi Image	Submenu see: Enroll Efi Image [▶ 66]
Device guard ready	
Remove 'UEFI CA' from DB	Submenu see: Remove UEFI CA from DB [▶ 67]
Restore DB defaults	Submenu see: Restore DB faults [▶ 67]
Secure Boot variables	Press enter key
PlatformKey(PK)	Press enter key
Key Exchange Keys	Press enter key
Authorized Signatures	Press enter key
Forbidden Signatures	Press enter key
Authorized TimeStamps	Press enter key
OsRecovery Signatures	Press enter key

8.5.1.3.1 Restore factory keys



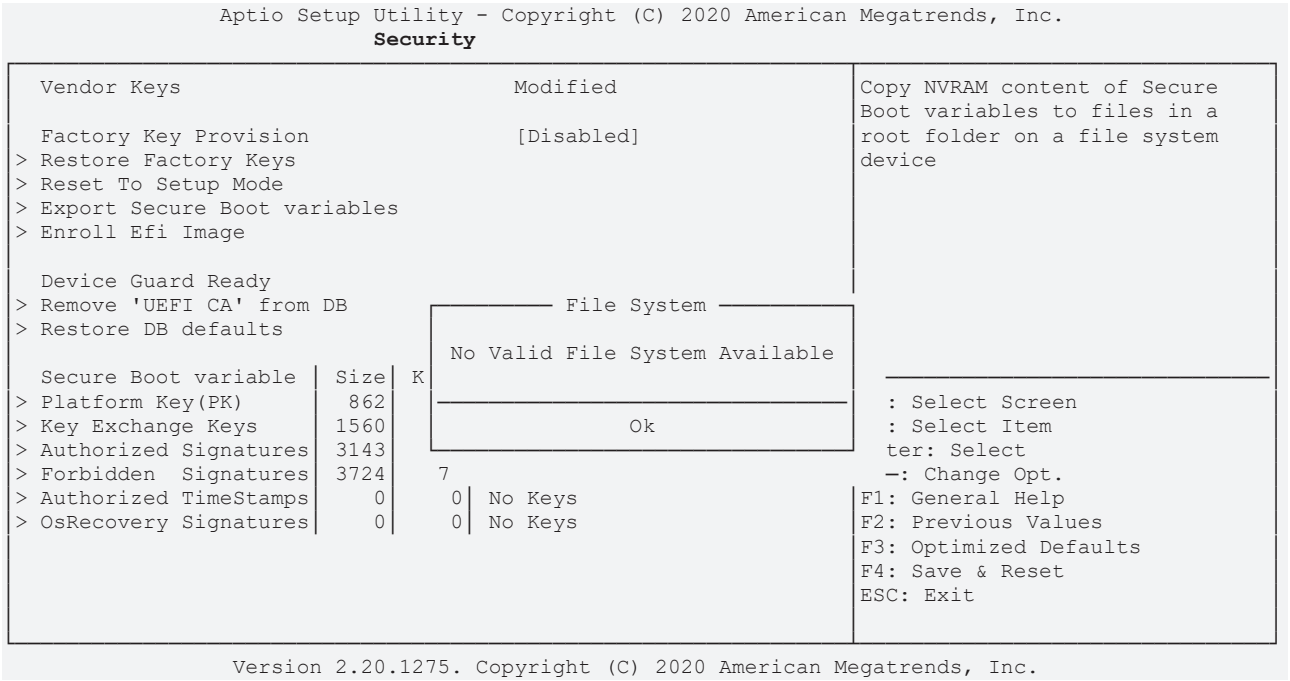
BIOS entry	Options
Vendor Keys	None
Restore factory keys	see box

8.5.1.3.2 Reset To Setup Mode



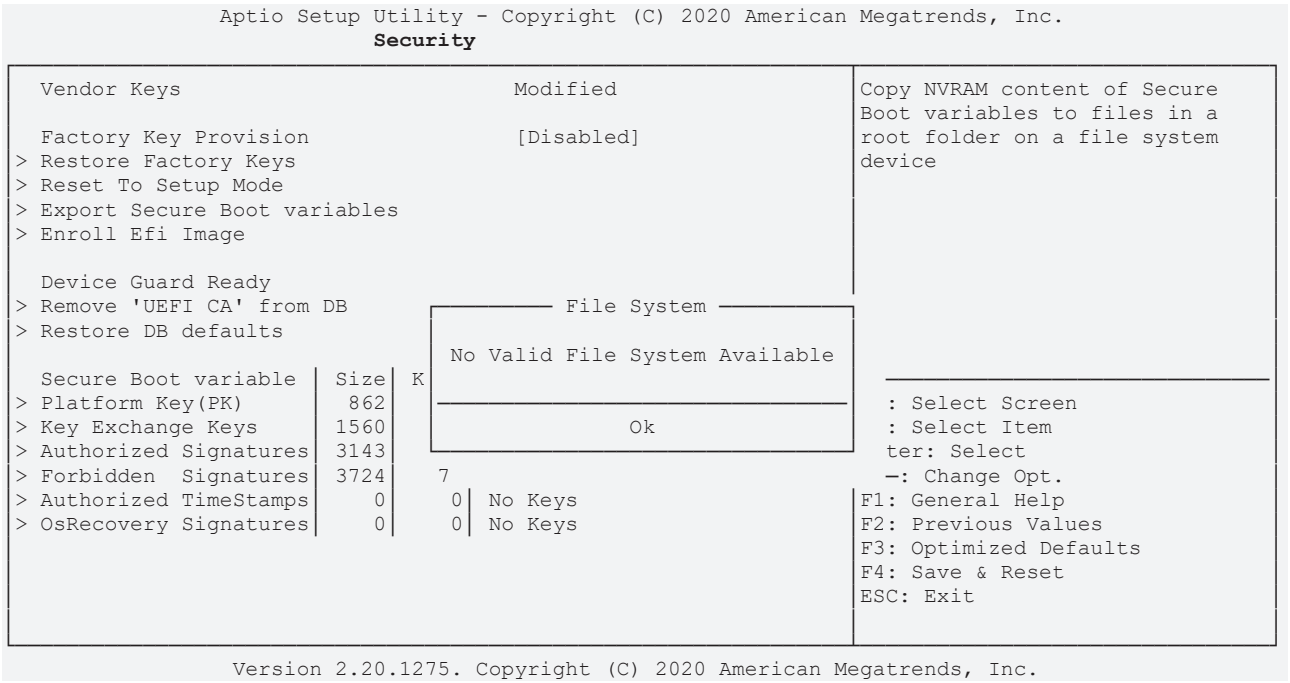
BIOS entry	Options
Vendor Keys	None
Restore To Setup Mode	see box

8.5.1.3.3 Export Secure Boot Variables



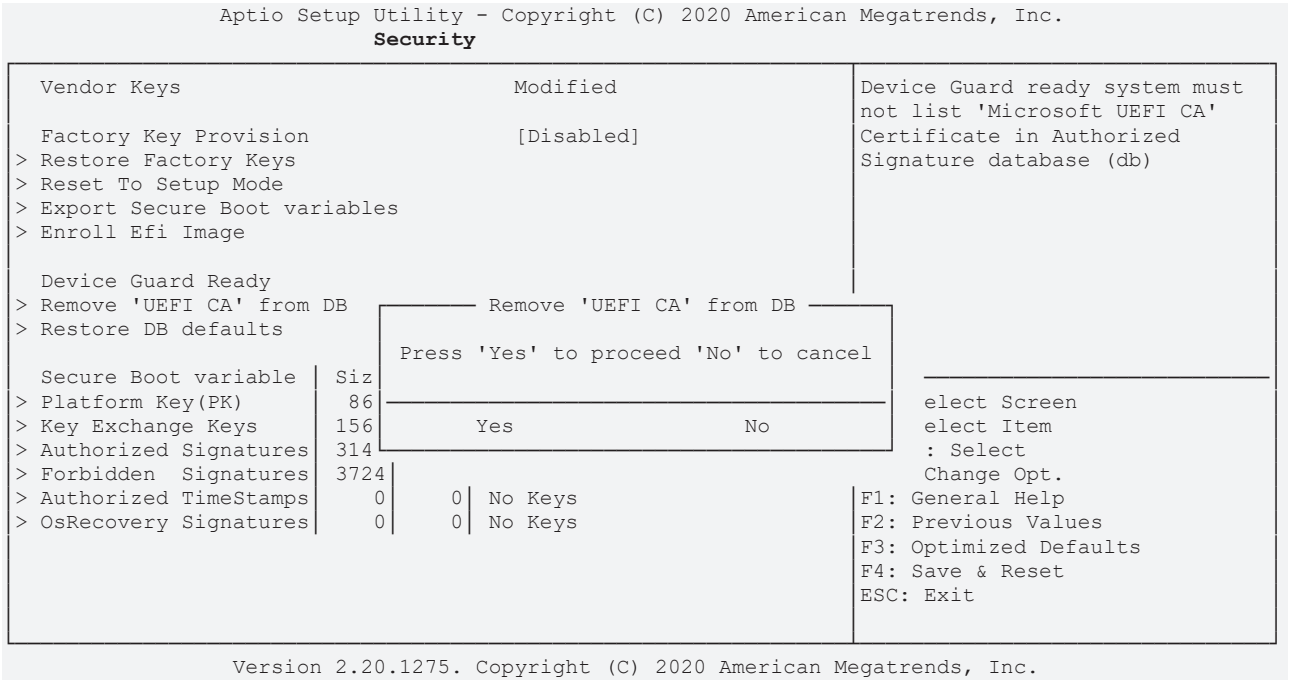
BIOS entry	Options
Vendor Keys	None
Export Secure Boot Variables	File system, see box

8.5.1.3.4 Enroll Efi Image



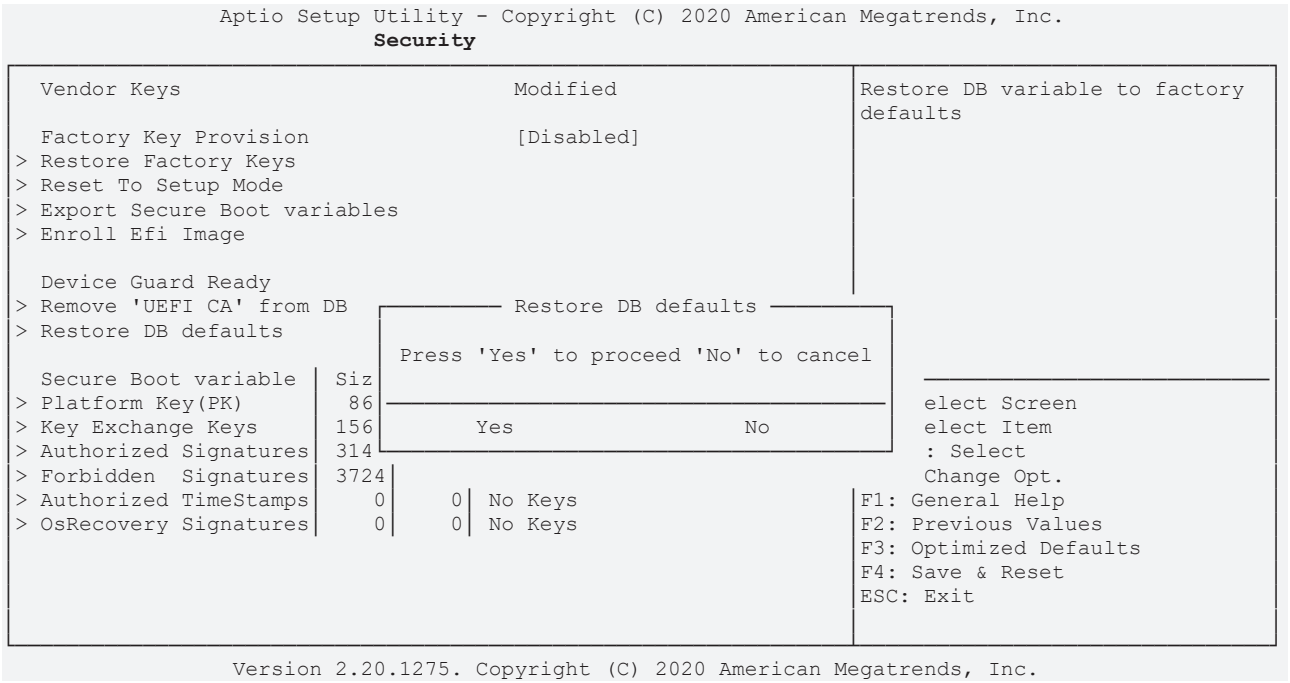
BIOS entry	Options
Vendor Keys	None
Enroll Efi Image	see box

8.5.1.3.5 Remove UEFI CA from DB



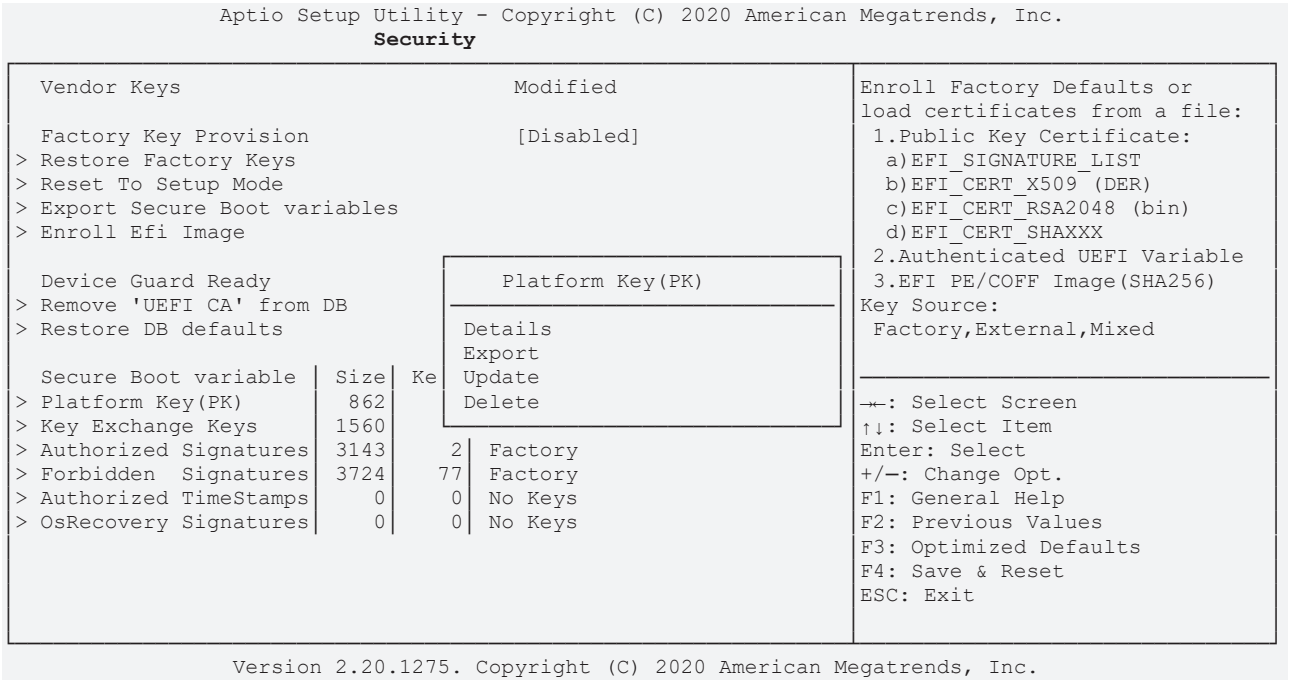
BIOS entry	Options
Vendor Keys	None
Remove ‘UEFI CA’ from DB	see box

8.5.1.3.6 Restore DB faults



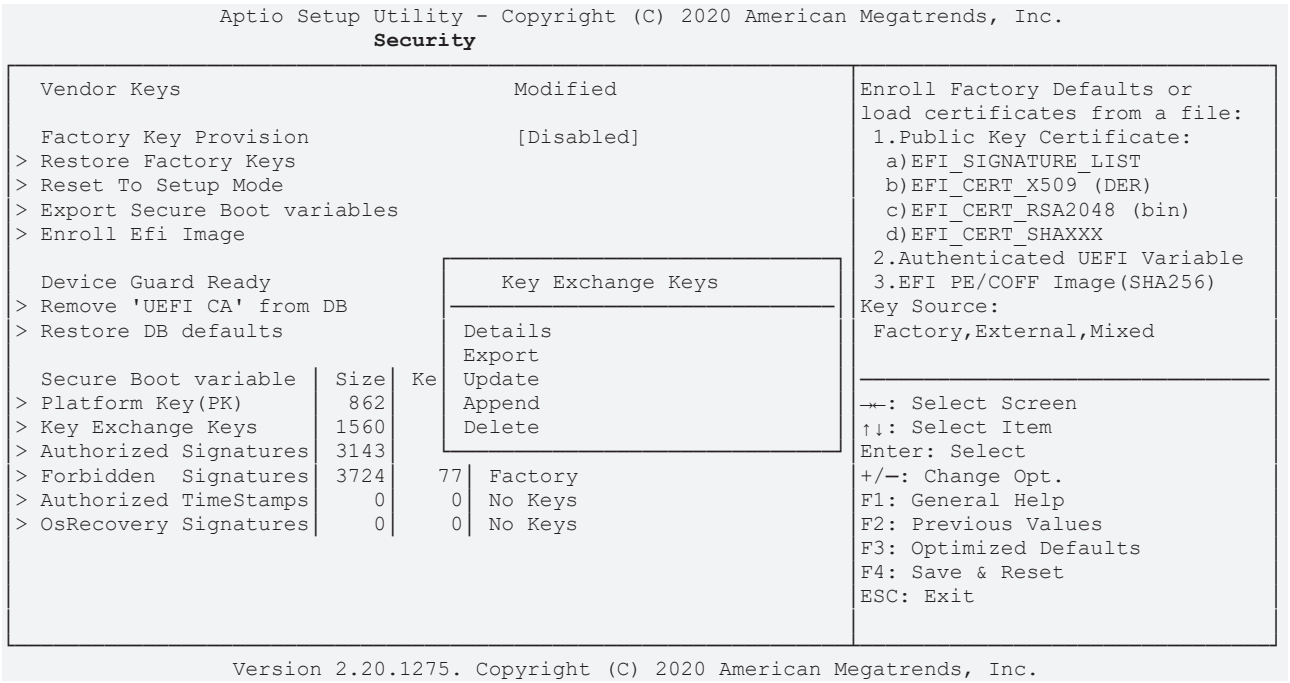
BIOS entry	Options
Vendor Keys	None
Restore DB faults	see box

8.5.1.3.7 Platform Key (PK)



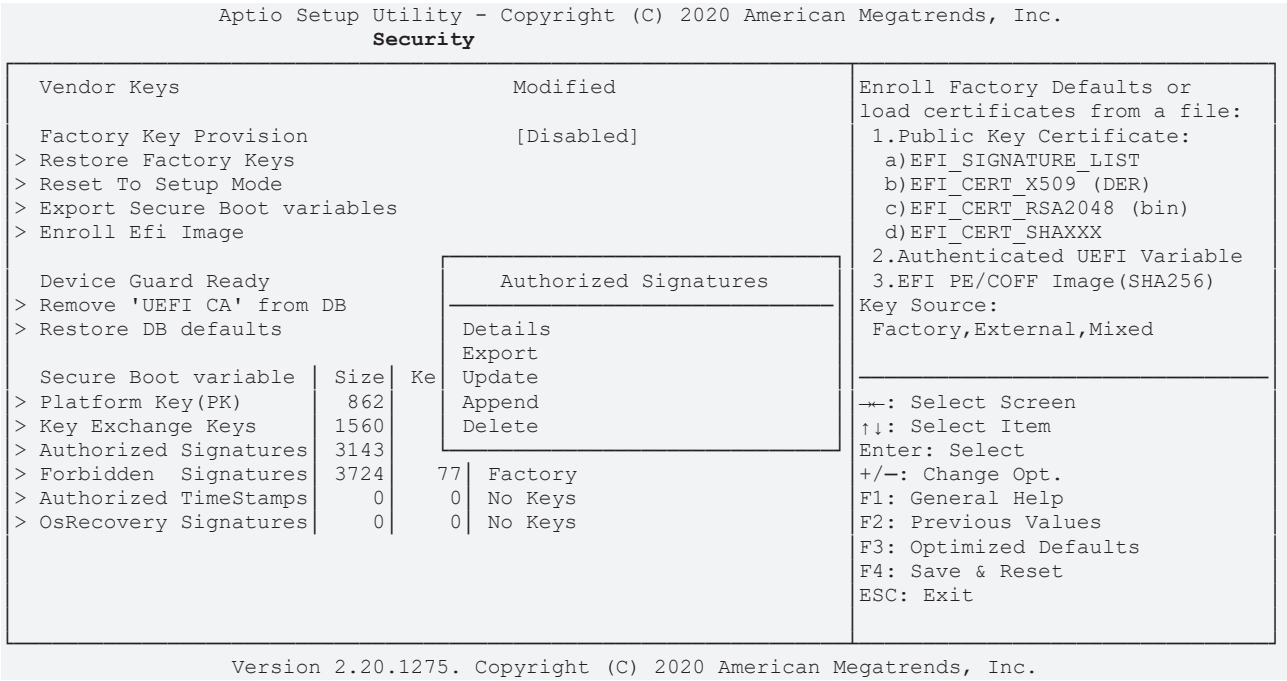
BIOS entry	Options
Vendor Keys	None
Platform Key (PK)	see box

8.5.1.3.8 Key Exchange Keys



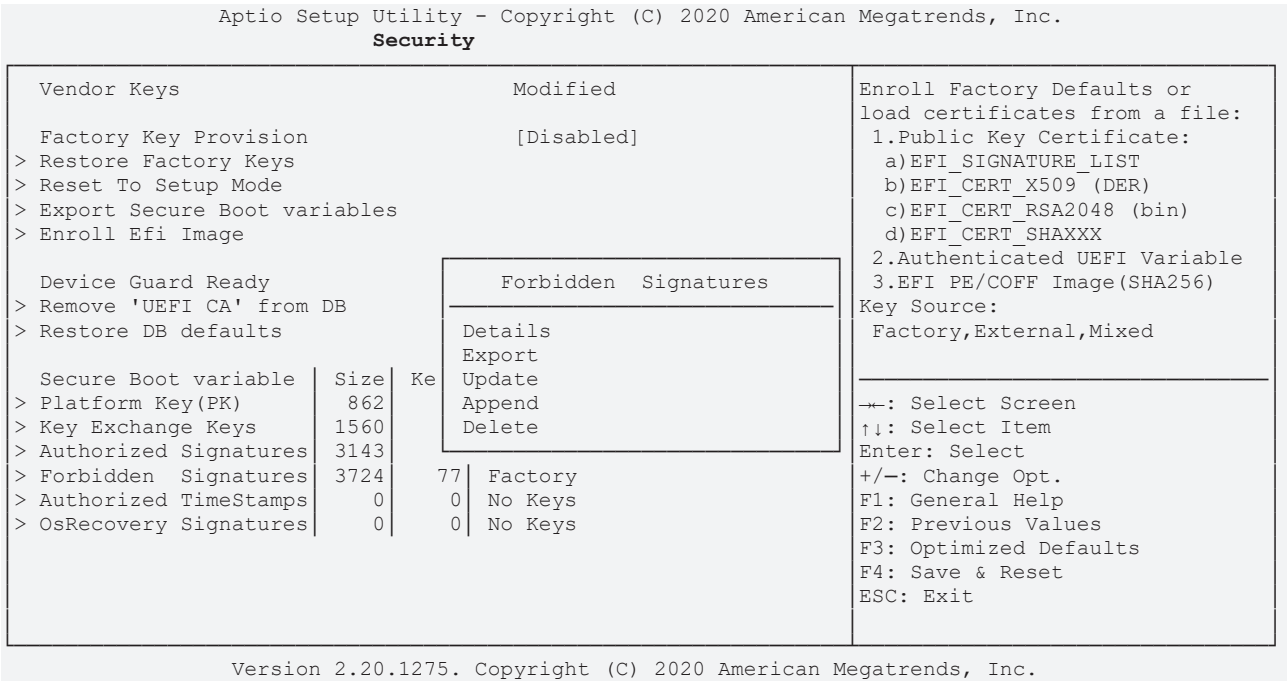
BIOS entry	Options
Vendor Keys	None
Key Exchange Keys	see box

8.5.1.3.9 Authorized Signatures



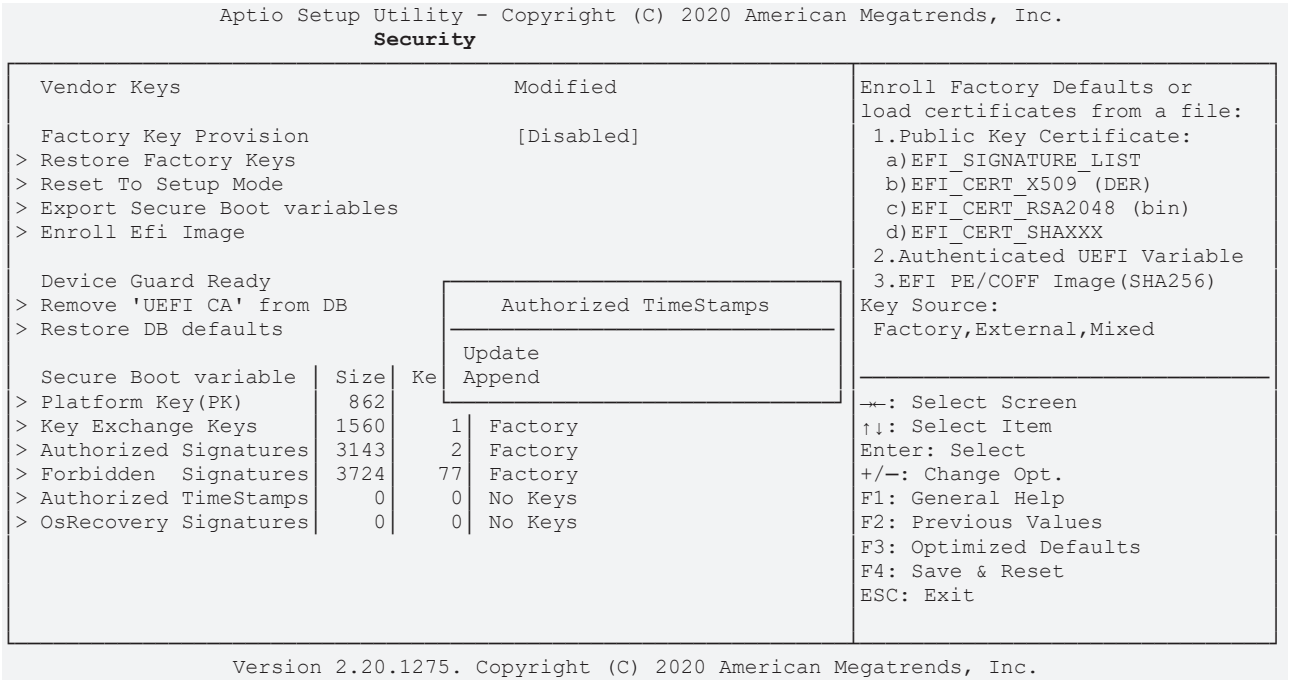
BIOS entry	Options
Vendor Keys	None
Authorized Signatures	see box

8.5.1.3.10 Forbidden Signatures



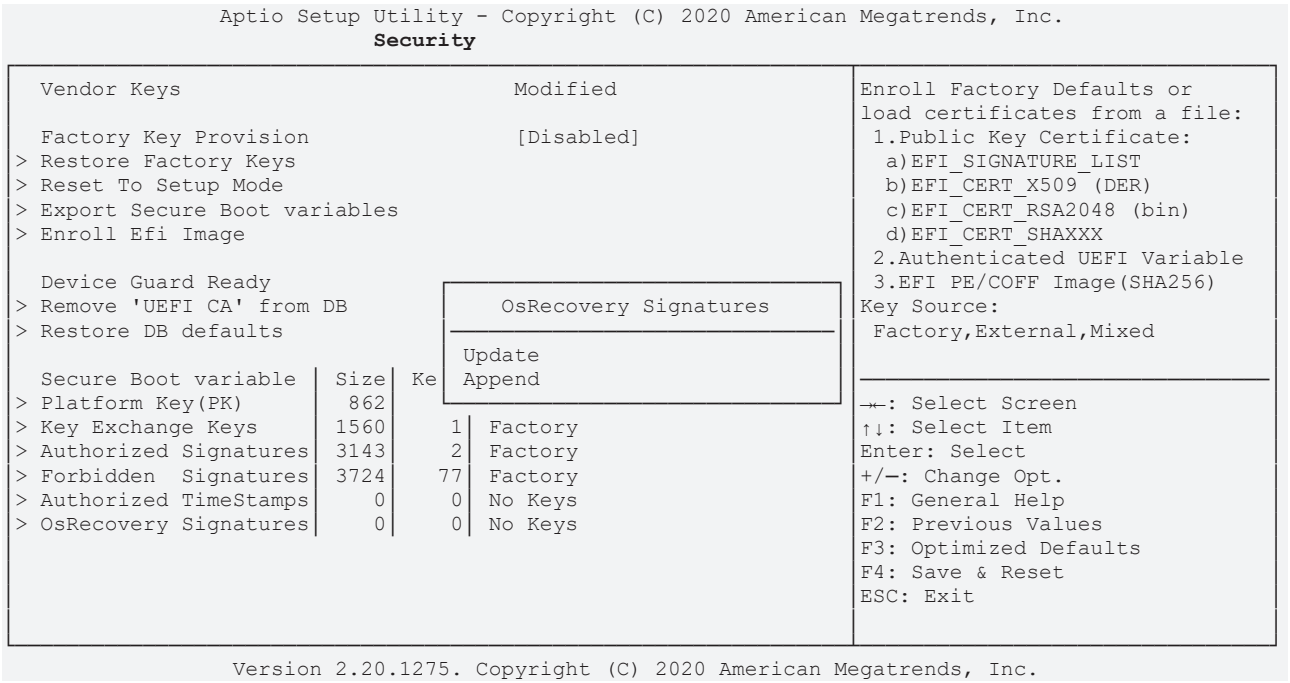
Bios entry	Options
Vendor Keys	None
Forbidden Signatures	see box

8.5.1.3.11 Authorized TimeStamps



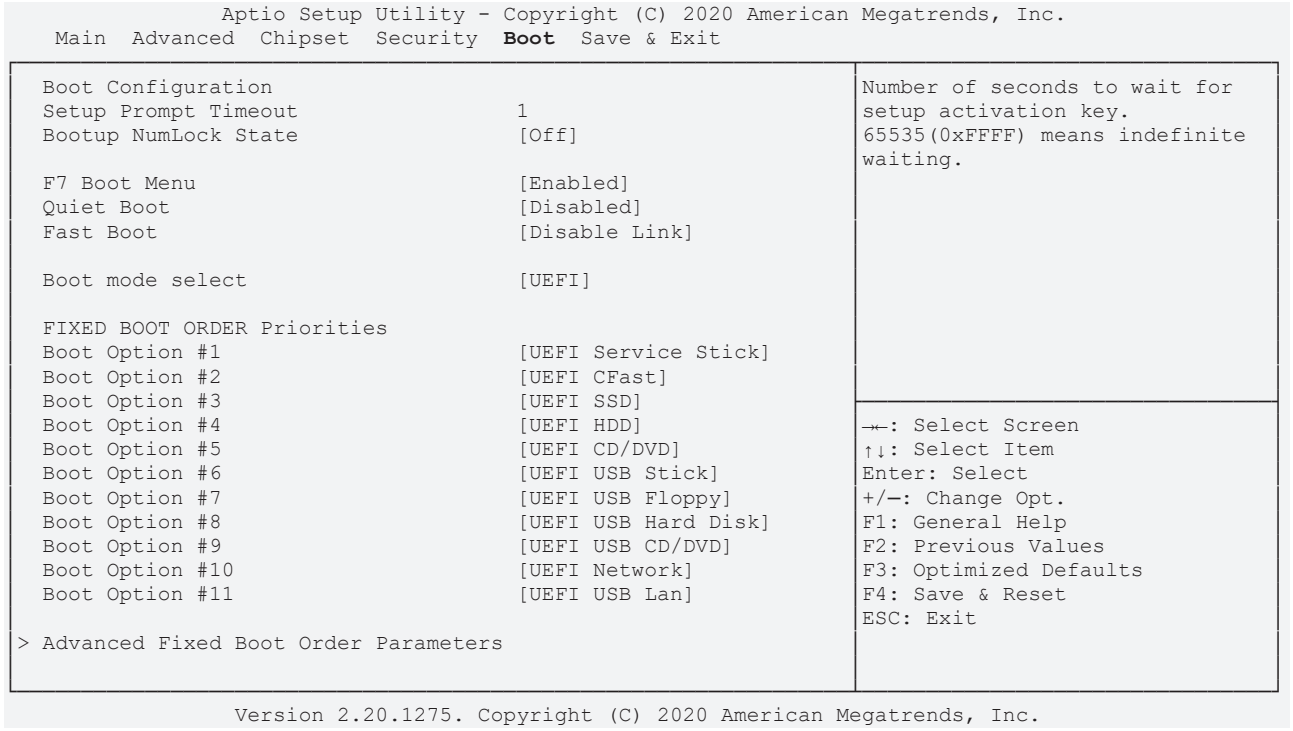
BIOS entry	Options
Vendor Keys	None
Authorized TimeStamps	see box

8.5.1.3.12 OsRecovery Signatures



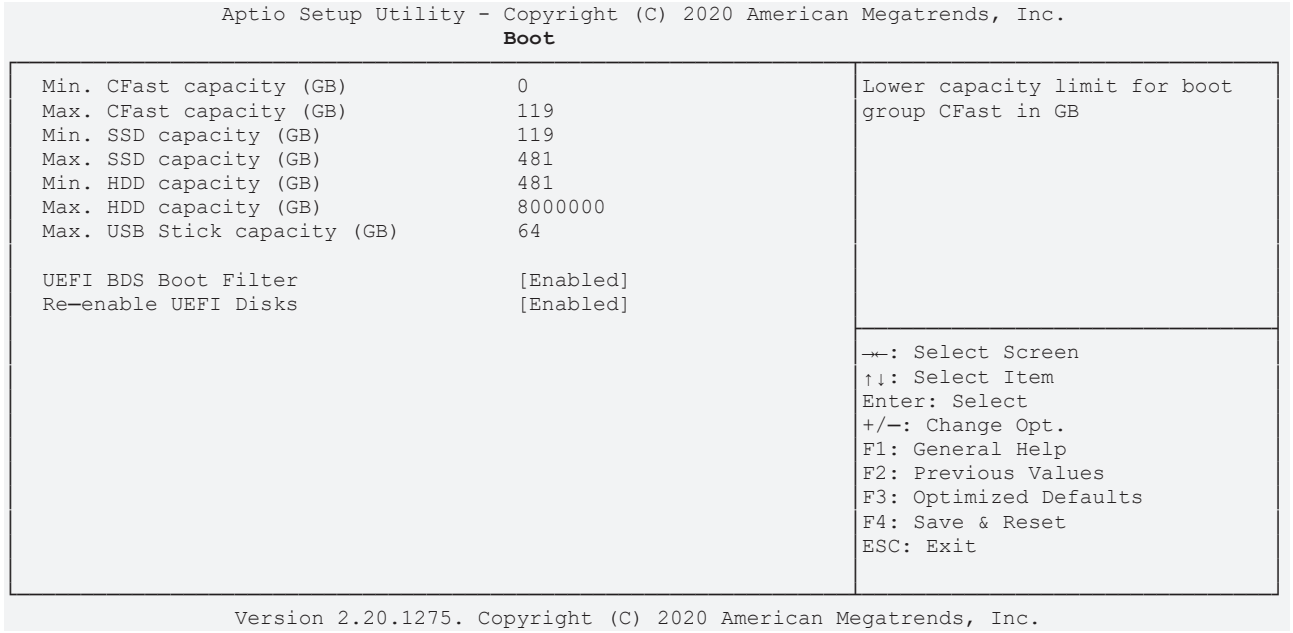
BIOS entry	Options
Vendor Keys	None
OsRecovery Signatures	see box

8.6 Boot



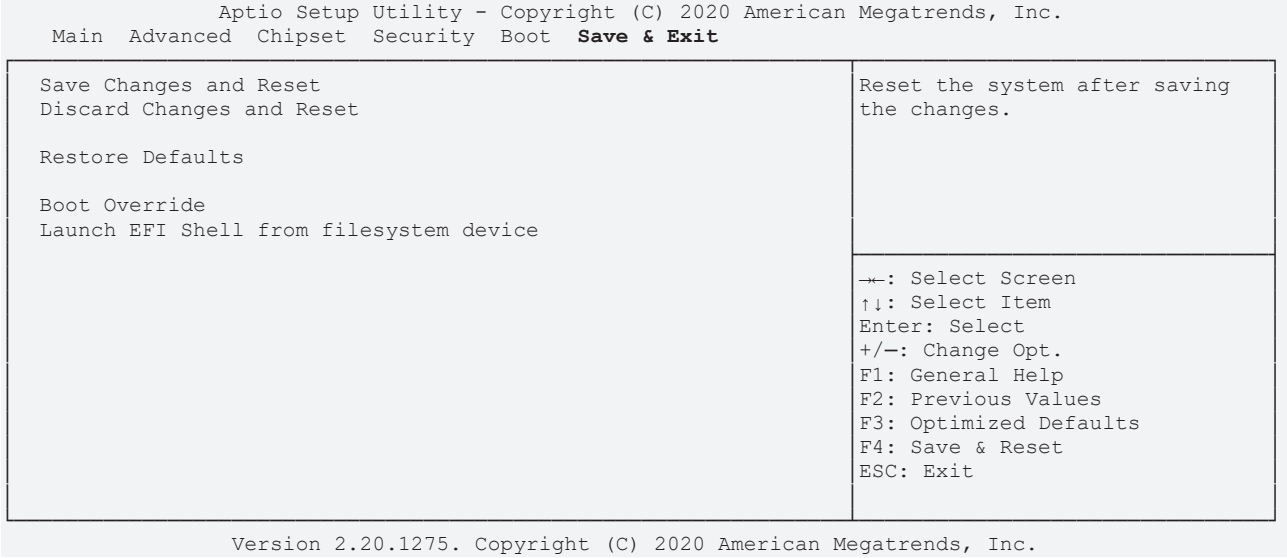
BIOS entry	Options
Boot Configuration	
Setup Prompt Timeout	None
Bootup NumLok state	On / Off
F7 Boot Menu	Enabled / Disabled
Quiet Boot	Enabled / Disabled
Fast boot	Disable Link / Enabled
Boot mode select	None
Fixed Boot Order Priorities	
Boot Option #1- #11	Here you can set the order of the boot media to be used.
Advanced Fixed Boot Order Parameters	Submenu see: Advanced Fixed Boot Order Parameters [▶ 72]

8.6.1 Advanced Fixed Boot Order Parameters



BIOS entry	Options
Min. CFast capacity (GB)	None
Max. CFast capacity (GB)	None
Min. SSD capacity (GB)	None
Max. SSD capacity (GB)	None
Min. HDD capacity (GB)	None
Max. HDD capacity (GB)	None
Max. USB Stick capacity (GB)	None
UEFI BDS Boot filter	Enabled / Disabled
Re-enable UEFI disks	Enabled / Disabled

8.7 Save&Exit



BIOS entry	Options
Save Changes and Reset	
Discard Changes and Reset	Press enter key
Restore defaults	Press enter key
Boot Override	
Launch EFI Shell from filesystem device	None

8.8 BIOS update

The "DecdFlsh" program and a bootable medium with the latest BIOS version are used if the BIOS needs to be updated. When doing this it is important to start the program from a DOS environment without a virtual memory manager such as "EMM386.EXE". If such a memory manager is loaded, the program will abort with an error message or cause a crash.

DecdFlsh is a program for the automatic updating of the BIOS on all boards with AMI-BIOS. All files contained in the zip file must be unpacked into a directory, from where

```
DecdFlsh Bios-Dateiname
```

calling takes place. The name of the BIOS file and its length are checked. The BIOS will now be programmed. DecdFlsh also exists as a UEFI tool for calling from the UEFI shell.

A running Flash procedure must never be interrupted, as otherwise the BIOS on the board will be destroyed. The Flash procedure takes about 75 seconds. The necessary firmware update takes place automatically.

Avoid damage due to incorrect update execution!

If the BIOS update is performed incorrectly, the board may become unusable. Therefore a BIOS update should only be done if the corrections / additions that the new BIOS version brings with it are really needed.

Before a planned BIOS update, it is essential to ensure that the BIOS file to be reloaded is really released for exactly this board and for exactly this board version. If an inappropriate file is used, the board will inevitably not boot afterwards.

9 Mechanical drawings

Dimensional notation

All dimensions are in mil (1 mil = 0.0254 mm). Data in square brackets are in mm.

9.1 PCB: Dimensions

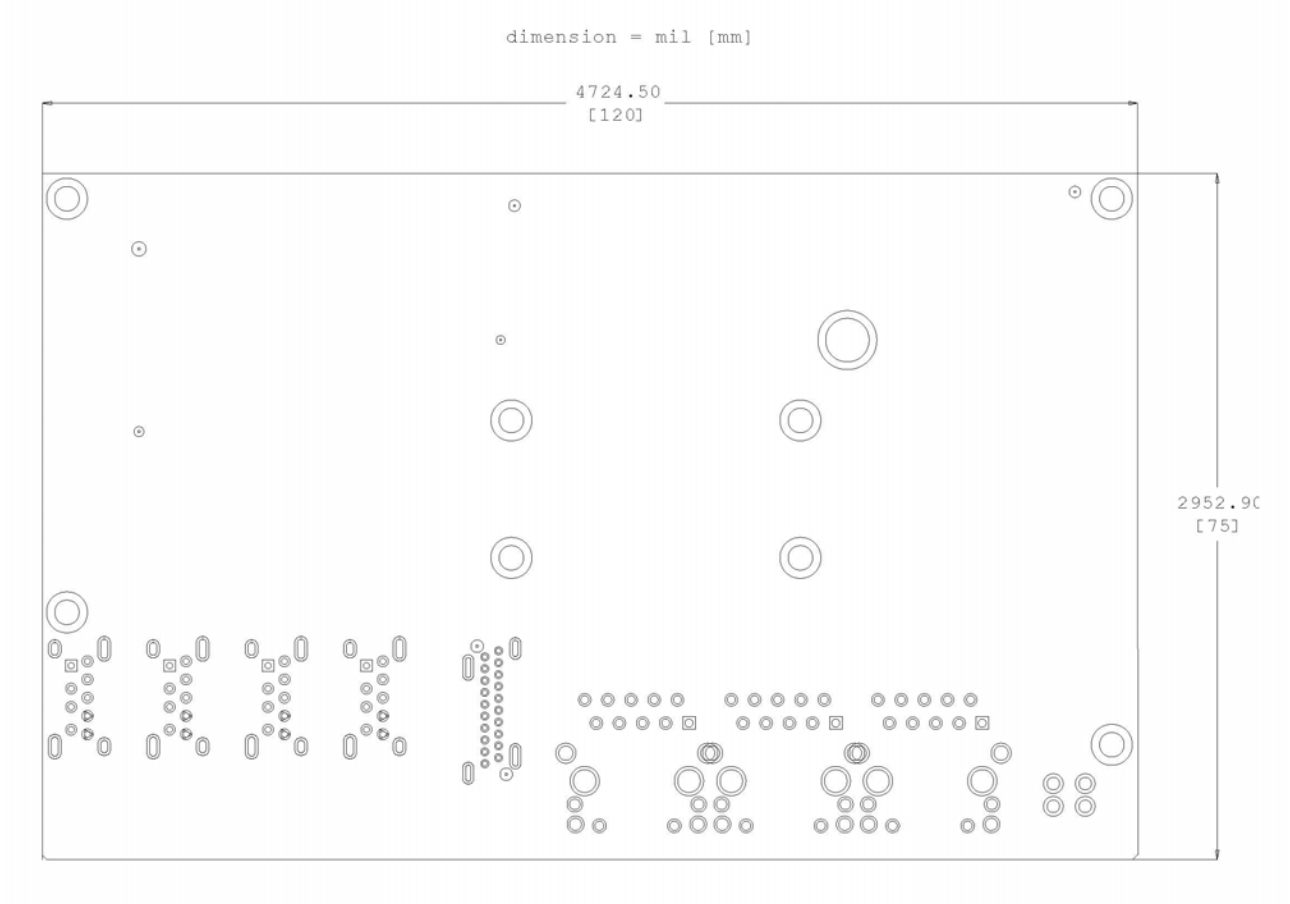


Fig. 16: CB7268 circuit board dimensions

9.2 PCB: Holes

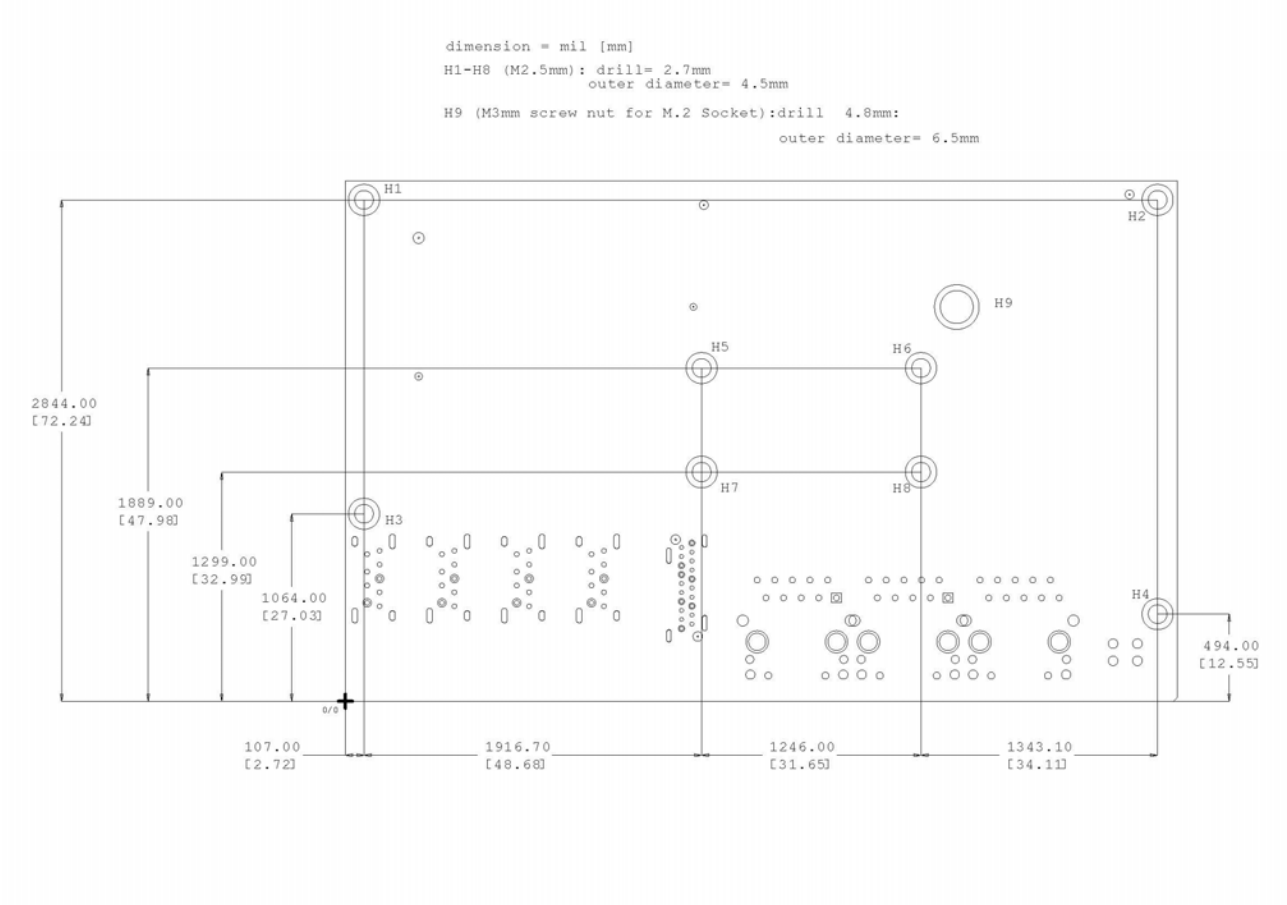


Fig. 17: CB7268 circuit board holes

10 Technical data

10.1 Electrical data

Power supply	
Board	24 V_{DC} power supply unit (+20 % / - 15 %)

Power	
transformer	45 W continuous load 70 W peak load

Current consumption	
RTC	≤ 10 µA

10.2 Environmental conditions

Temperature range	
Operating	0 °C to +60 °C (extended temperature range on request)
Storage	-25 °C to +85 °C
Dispatch	-25 °C to +85 °C, for packed boards

Temperature changes	
Operating	0.5 °C per minute, 7.5 °C in 30 minutes
Storage	1.0 °C per minute
Dispatch	1.0 °C per minute, for packed boards

Relative humidity	
Operating	5% to 85% (non-condensing)
Storage	5% to 95% (non-condensing)
Dispatch	5% to 100% (non-condensing), for packed boards

Impact	
Operating	150 m/s², 6 ms
Storage	400 m/s², 6 ms
Dispatch	400 m/s², 6 ms, for packed boards

Vibrations	
Operating	10 to 58 Hz, amplitude 0.075 mm 58 to 500 Hz, 10 m/s²
Storage	5 to 9 Hz, amplitude 3.5 mm 9 to 500 Hz, 10 m/s²
Dispatch	5 to 9 Hz, 3.5 mm amplitude 9 to 500 Hz, 10 m/s², for packed boards

Note on impact and vibration resistance

The specifications for impact and vibration resistance refer only to the motherboard itself without heat sink, memory module, cabling, etc.

10.3 Thermal specifications

The board is specified for an ambient temperature range of 0 °C to +60 °C (extended temperature range on request). In addition, care must be taken that the temperature of the processor die does not exceed 110 °C. To ensure this a suitable cooling concept must be implemented that is oriented to the maximum power consumption of the processor/chipset. It must also be ensured that any existing controllers are included in the cooling concept. The power consumption of these function blocks may be of the same order of magnitude as the power consumption of the processor.

The board is prepared with suitable holes for the use of modern cooling solutions. We have a series of compatible cooling components in our range. Your distributor will be pleased to assist you in selecting suitable solutions.

NOTE

Prevent the maximum die temperature being exceeded!

It is the end customer's responsibility to ensure that the die temperature of the processor does not exceed 110 °C! Continuous overheating can destroy the board!

If the temperature exceeds 110 °C, the ambient temperature needs to be reduced. Ensure sufficient air circulation if necessary.

11 Support and Service

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You will also find further documentation for Beckhoff components there.

12 Appendix I: Post Codes

During the boot phase, the BIOS generates a series of status messages (so-called "POST Codes"), which can be output with the help of a suitable reading device (POST Code card). The meanings of the POST Codes are explained in the document "Aptio™ 5.x Status Codes" from American Megatrends®, which is available from the website http://www.ami.com. In addition, the following OEM POST Codes are output:

Code	Description
87h	BIOS-API started
88h	PCA9535 started
89h	PWRCTRL firmware started

13 Appendix II: Resources

13.1 Interrupt CB7268

The system BIOS determines the interrupt requests (IRQs) for all devices that request interrupts. In the operating system, interrupts can be dynamically forwarded to IRQs and can support a reassignment of IRQs if there is a conflict with the current use of the interrupt.

For further information please refer to the chipset manual.

13.2 PCI devices CB7268

The PCI devices listed here all exist on the board, including those that are detected and configured by the BIOS. Due to the BIOS setup settings it may be the case that various PCI devices or functions of devices are not activated. If devices are deactivated, the bus numbers of other devices may change as a result.

Bus	Dev.	Fct.	Controller / Slot
00	00	00	Host bridge ID 3E35
00	02	00	VGA controller ID 3EA0
00	04	00	Data acquisition/signal processing controller ID 1903
00	08	00	System device ID 1911
00	12	00	Data acquisition/signal processing controller ID 9DF9
00	14	00	XHCI USB controller ID 9DED
00	14	02	RAM controller ID 9DEF
00	16	00	Communication device ID 9DE0
00	17	00	RAID controller ID 282A
00	1C	00	PCI-to-PCI bridge (PCIE) ID 9DB8
00	1C	07	PCI-to-PCI bridge (PCIE) ID 9DBF
00	1D	00	PCI-to-PCI bridge (PCIE) ID 9DB0
00	1D	03	PCI-to-PCI bridge (PCIE) ID 9DB3
00	1F	00	ISA bridge ID 9D84
00	1F	03	HD audio device ID 9DC8
00	1F	04	SMBus controller ID 9DA3
00	1F	05	Controller ID 9DA4
00	1F	06	Ethernet controller ID 15BD
02	00	00	Ethernet controller (PCIE) ID 1533
03	00	00	Mass storage controller (PCIE) ID 5008
04	00	00	Ethernet controller (PCIE) ID 1533

13.3 SMB devices CB7268

The following table lists the reserved SM-Bus device addresses in 8-bit notation.

NOTE

These address ranges may not be used by external devices even if the component assigned in the table doesn't exist on the motherboard.

Address	Function
B0, B2, B8, BA	PWCTR3
70, 72	PostCode
34 (old B4)	CA2000-0021/23 (power supply unit)
40	PCA9535BS (16-bit I2C and SMBus, low power I/O port with interrupt)
..	SUSV

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