BECKHOFF New Automation Technology

Original Manual for | EN

CB1067

Computerboard

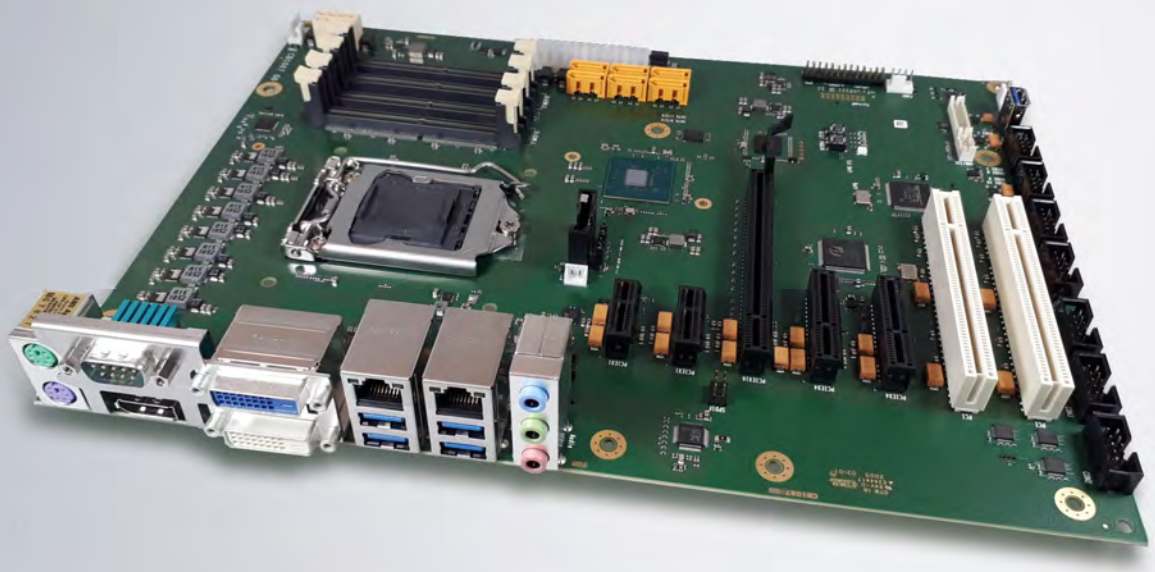

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Table of Contents

1 Documentation issue status

Version	Modifications
0.1	First preliminary version, G0
0.2	Preliminary version G0 with BIOS 0.11
1.0	First release G2, with current BIOS 0.13 and new title page.
1.1	G2, BIOS Version a.020 added.
1.2	Information for real-time applications added

2 Notes on the documentation

This description is only intended for the use of trained specialists in control and automation engineering who are familiar with the applicable national standards.
It is essential that the documentation and the following notes and explanations are followed when installing and commissioning the components.
It is the duty of the technical personnel to use the documentation published at the respective time of each installation and commissioning.

The responsible staff must ensure that the application or use of the products described satisfy all the requirements for safety, including all the relevant laws, regulations, guidelines and standards.

Disclaimer

The documentation has been prepared with care. The products described are, however, constantly under development.
We reserve the right to revise and change the documentation at any time and without prior announcement.
No claims for the modification of products that have already been supplied may be made on the basis of the data, diagrams and descriptions in this documentation.

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Patent Pending

The EtherCAT Technology is covered, including but not limited to the following patent applications and patents:
EP1590927, EP1789857, EP1456722, EP2137893, DE102015105702
with corresponding applications or registrations in various other countries.

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3 Safety instructions

Safety regulations

Please note the following safety instructions and explanations!
Product-specific safety instructions can be found on following pages or in the areas mounting, wiring, commissioning etc.

Exclusion of liability

All the components are supplied in particular hardware and software configurations appropriate for the application. Modifications to hardware or software configurations other than those described in the documentation are not permitted, and nullify the liability of Beckhoff Automation GmbH & Co. KG.

Personnel qualification

This description is only intended for trained specialists in control, automation and drive technology who are familiar with the applicable national standards.

Description of symbols

In this documentation the following symbols are used with an accompanying safety instruction or note. The safety instructions must be read carefully and followed without fail!

⚠ DANGER

Serious risk of injury!

Failure to follow the safety instructions associated with this symbol directly endangers the life and health of persons!

⚠ WARNING

Risk of injury!

Failure to follow the safety instructions associated with this symbol endangers the life and health of persons!

⚠ CAUTION

Personal injuries!

Failure to follow the safety instructions associated with this symbol can lead to injuries to persons!

NOTE

Damage to the environment or devices

Failure to follow the instructions associated with this symbol can lead to damage to the environment or equipment.

Tip or pointer

This symbol indicates information that contributes to better understanding.

UL note

This symbol indicates important information regarding UL certification.

Intended use

The CB1067 Computer Board was designed and developed exclusively for configuration in automation processes. To that end the board is equipped with external interfaces in order to acquire or output digital or analog signals or forward them to higher-level components.

Any other use is regarded as inappropriate.

The specified limits for electrical and technical data must be adhered to.

4 Overview

4.1 Properties

The CB1067 is an industrial motherboard in the ATX form factor. It is based on Intel®'s current Coffeelake (Refresh) S-processors of the Core™, Celeron™ and Pentium™ families in the 8th and 9th generation in connection with the Q370-PCH chipset. Using its four SO-DIMM260 slots it can be equipped with up to 128 GB of DDR4-2666 memory. With two PCI, two PCIe x1, two PCIe x4 and one PCIe x16 slots, the board offers comprehensive expansion options. A large number of internal and external connections make the CB1067 a highly universally usable motherboard. The connections are rounded off by four serial interfaces, two Gigabit-LAN connections, various analog and digital sound inputs and outputs, 13 USB interfaces, DVI/ HDMI and DisplayPort connection as well as six 6G-capable SATA connections.

Furthermore, the board serves via the integrated Trusted Platform Module (TPM) as a Trusted Computing Platform and thus offers basic safety functions.

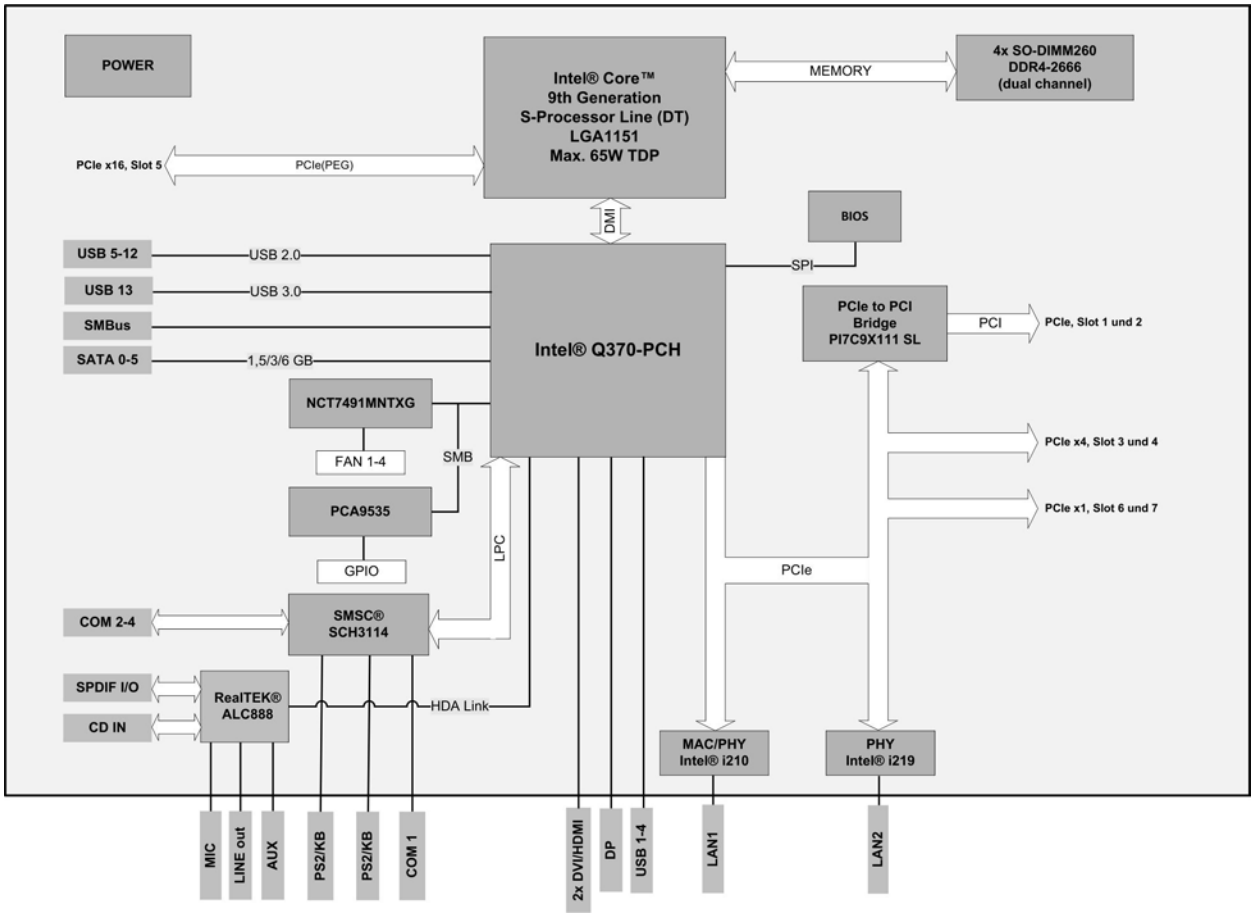


Fig. 1: CB1067-Block diagram

4.2 List of features

CB1067	ATX board
CPU	Intel® Core™ i3 / Core™ i5 / Core™ i7 Intel® Pentium® Intel® Celeron®
Chipset	Intel® Q370-PCH
Socket	LGA 1151
Memory	4x DDR4@2666 MHz, 32 GB each, SODIMM260 (NonECC), total memory capacity up to 128 GB
I/O external	2x MINIDIN6 (mouse & keyboard) 1x COM 1x DP 1.2 2x DVI-D (DVI or HDMI 1.4) 4x USB3.1 Gen2 2x GBit LAN, Intel® i219 and i210 3x jacks 3.5 mm (mic, line out, aux)
I/O internal	3x COM 6x SATA 3.0, RAID 0/1/5/10 2x PCI32 slots 2x PCIe x1 (3.0) + 2x PCIe x4 (3.0) + 1x PCIe x16 (3.0) 8x USB 2.0 8x GPIO 4x fans (of which 3 are controlled fans) 1x SMB connection
Graphic resolution	DisplayPort1.2: 4096x2304@60 Hz HDMI1.4: 4096x2160@30 Hz
RTC	Internal or external CMOS battery
BIOS	AMI® Aptio V
Power supply	Standard ATX PSU
Format	ATX (305 x 220 mm)

Availability of the processors

The list of features lists all the processors that can be ordered. Their actual availability depends on the manufacturer.

4.3 Specifications and documents

The following documents, specifications or webpages were used for the preparation of this manual or as further technical documentation respectively.

- **PCI specification**
- Version 2.3 or 3.0
- www.pcisig.com
- **PCI Express® Base Specification**
- Version 5.0
- www.pcisig.com
- **ACPI specification**
- Version 5.0
- www.acpi.info
- **ATA/ATAPI specification**
- Version 7 Rev. 1
- www.t13.org
- **USB specifications**
- www.usb.org
- **SM-Bus specification**
- Version 2.0
- www.smbus.org
- **Intel® chip descriptions**
- Intel® Core™ processor product family data sheet
- www.intel.com
- **Intel® chip description**
- i219 data sheet
- i210 datasheet
- www.intel.com
- **SMSC® chip description**
- SCH3114 datasheet (NDA required)
- www.smsc.com
- **American Megatrends®**
- Aptio™ Text Setup Environment (TSE) User Manual
- www.ami.com
- **American Megatrends®**
- Aptio™ 5.x Status Codes
- www.ami.com

5 Connections

All connections (internal and external) on the CB1067 are described on the following pages.

NOTE

Requirement for the cabling

The cables used must meet certain requirements for most interfaces. For example, twisted and shielded cables are necessary for a reliable USB 2.0 connection. Limitations in the maximum cable length are also no rarity. All of these interface-specific requirements can be found in the respective specifications and you should observe them accordingly.

5.1 Plug connector overview

The following illustration provides an overview of the plug connections on the CB1067 board. The function of the respective connector can be taken from the table below. The listed page in the manual provides you with further information on this connection. The interfaces are described clockwise, beginning with the PS/2 mouse and keyboard (P1601).

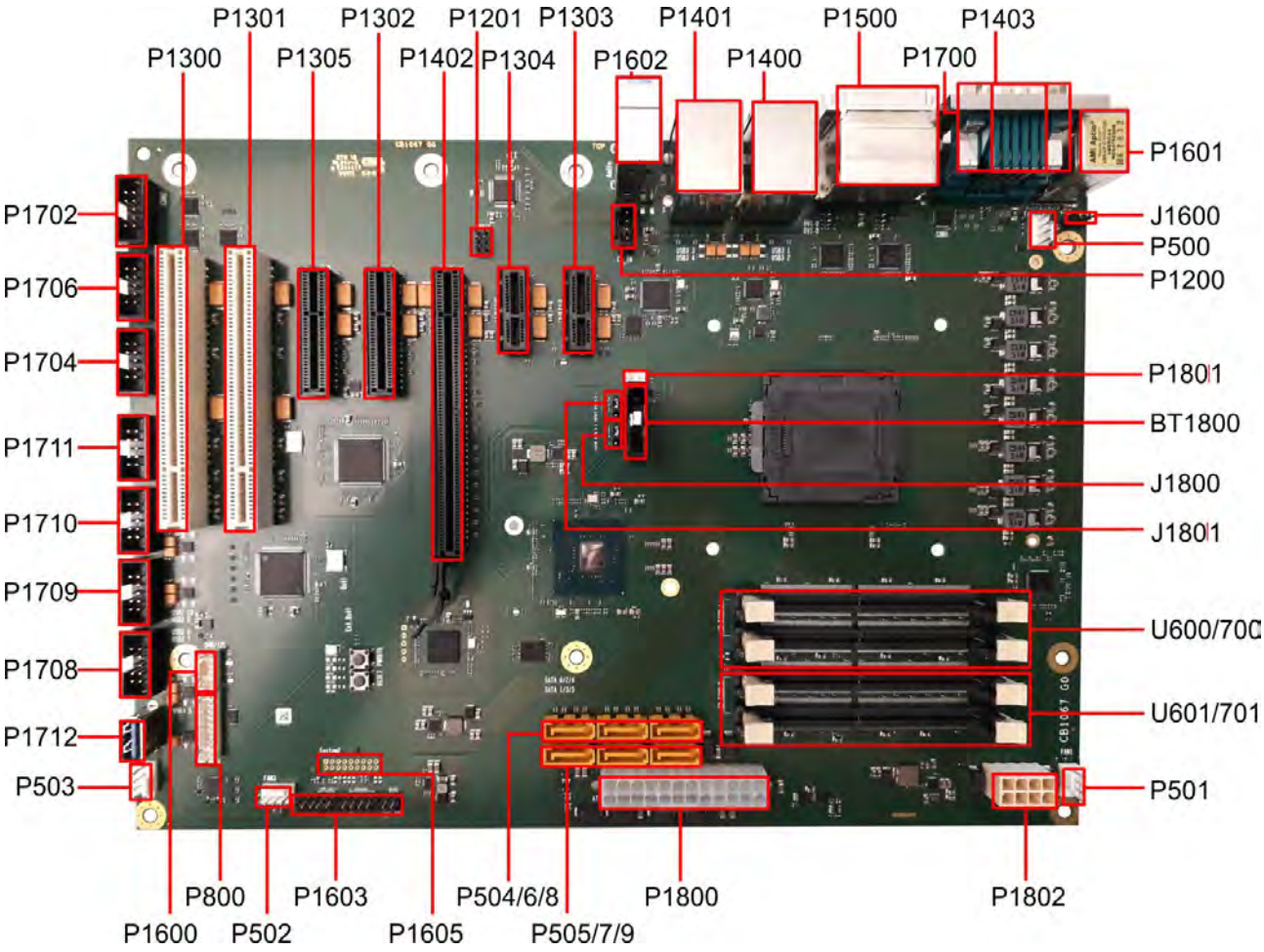


Fig. 2: CB1067 connector overview

Number	Function (designation)	Page
P1601	PS/2 mouse and keyboard	PS/2 mouse and keyboard (P1601) [▶ 14]
J1600	Jumper Keyboard Power (KBPWR)	Jumper Keyboard Power KBPWR (J1600) [▶ 14]
P500	4-pin connector (FAN2/CPU)	FAN 1 – 4 (P500/1/2/3) [▶ 15]
P1200	4-pin connector (CD-In)	CD-In (P1200) [▶ 16]
P1801	2-pin connector (battery)	Battery (BT1800/P1801) [▶ 16]
BT1800	Battery holder for CR2032	Battery (BT1800/P1801) [▶ 16]
J1800	Jumper Clear CMOS 1	Clear CMOS (J1800/1801) [▶ 17]
J1801	Jumper Clear CMOS 2	Clear CMOS (J1800/1801) [▶ 17]
U600/700	SO-DIMM260 A1 and A2	Memory SO-DIMM260 (U600/700 and U601/701) [▶ 17]
U601/701	SO-DIMM260 B1 and B2	Memory SO-DIMM260 (U600/700 and U601/701) [▶ 17]
P501	4-pin connector (FAN1)	FAN 1 – 4 (P500/1/2/3) [▶ 15]
P1802	2x4-pin connector MiniFit 12 V	Power supply (P1800 and P1802) [▶ 21]
P1800	2x12-pin connector ATX Power	Power supply (P1800 and P1802) [▶ 21]
P505/7/9	SATA 1/3/5	SATA (P504 - P509) [▶ 22]
P504/6/8	SATA 0/2/4	SATA (P504 - P509) [▶ 22]
P1605	2x9-pin system	Connector System 1 (P1603) [▶ 22]
P1603	2x13-pin connector ATX Bh system	Connector System 1 (P1603) [▶ 22]
P502	4-pin connector (FAN3)	FAN 1 – 4 (P500/1/2/3) [▶ 15]
P800	2x5-pin connector GPIO	GPIO (P800) [▶ 23]
P1600	2x10-pin connector SMB/I²C	SMB/I²C (P1600) [▶ 23]
P503	4-pin connector FAN4	FAN 1 – 4 (P500/1/2/3) [▶ 15]
P1712	USB 3.1 Gen2	USB 3.0 type A (P1712) [▶ 24]
P1708	2x5-pin connector USB 2.0, 7 - 8	USB 2.0 (P1708 - 1711) [▶ 25]
P1709	2x5-pin connector USB 2.0, 9 - 10	USB 2.0 (P1708 - 1711) [▶ 25]
P1710	2x5-pin connector USB 2.0, 11 - 12	USB 2.0 (P1708 - 1711) [▶ 25]
P1711	2x5-pin connector USB 2.0, 13 - 14	USB 2.0 (P1708 - 1711) [▶ 25]
P1704	2x5-pin connector COM 4	Serial interfaces COM2/3/4 (P1702/P1704/P1706) [▶ 26]
P1706	2x5-pin connector COM 3	Serial interfaces COM2/3/4 (P1702/P1704/P1706) [▶ 26]
P1702	2x5-pin connector COM 3	Serial interfaces COM2/3/4 (P1702/P1704/P1706) [▶ 26]
P1300	PCI socket	PCI interfaces (P1300 and P1301) [▶ 27]
P1301	PCI socket	PCI interfaces (P1300 and P1301) [▶ 27]
P1305	PCIe x4 socket	PCI-Express interfaces x4 (P1305 and P1302) [▶ 30]
P1302	PCIe x4 socket	PCI-Express interfaces x4 (P1305 and P1302) [▶ 30]
P1402	PCIe x16 socket	PCI-Express interface x16 (P1402) [▶ 31]
P1201	2x3-pin connector SPDIF	SPDIF connector (P1201) [▶ 34]
P1304	PCIe x1 socket	PCI-Express x1 (P1304 and P1303) [▶ 35]
P1303	PCIe x1 socket	PCI-Express x1 (P1304 and P1303) [▶ 35]

Number	Function (designation)	Page
P1602	3x 3.5 mm jack	Audio connections (P1602) [▶ 35]
P1401	LAN 1GB + USB3.1 Gen2	LAN and USB 3.0 (P1401 and P1400) [▶ 36]
P1400	LAN 1GB + USB3.1 Gen2	LAN and USB 3.0 (P1401 and P1400) [▶ 36]
P1500	DVI-D	DVI-D (P1500) [▶ 37]
P1700	COM 1	Serial interface COM1 and DP/HDMI/DVI (P1700 and P1403) [▶ 38]
P1403	DP / HDMI / DVI	Serial interface COM1 and DP/HDMI/DVI (P1700 and P1403) [▶ 38]

5.2 PS/2 mouse and keyboard (P1601)

PS/2 mice and keyboards can be connected using standard Mini DIN connectors. In addition to the normal power supply (VCC), these components can also be supplied with power via the standby voltage (SVCC), so that you can wake the board from the standby or suspend mode with the mouse or keyboard. To activate this option, set the KBPWR jumper accordingly. Also make the necessary settings in the BIOS setup.

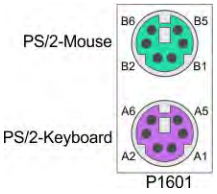


Fig. 3: PS/2 connector

Pin assignment of PS/2 mouse					
Description	**Name**	**Pin**		**Name**	**Description**
Mouse Data	MDAT	B1	B2	N/C	Reserved
Ground	GND	B3	B4	(S)VCC	5 V supply voltage
Mouse Clock	MCLK	B5	B6	N/C	Reserved

Pin assignment of PS/2 keyboard

Pin assignment of PS/2 keyboard					
Description	**Name**	**Pin**		**Name**	**Description**
Keyboard data	KDAT	A1	A2	MDAT	Mouse Data
Ground	GND	A3	A4	(S)VCC	5 V supply voltage
Keyboard Clock	KCLK	A5	A6	MCLK	Mouse Clock

5.3 Jumper Keyboard Power KBPWR (J1600)

PS/2 mouse and keyboard are supplied with power either via the normal supply voltage VCC or via the standby voltage SVCC. The voltage you choose depends on the setting of the KBPWR jumper. If contacts 1 and 2 are closed, then VCC is applied; if contacts 2 and 3 are closed, then SVCC.

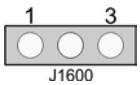


Fig. 4: KBPWR jumper

5.4 FAN 1 – 4 (P500/1/2/3)

The module has four 4-pin fan connections, with which you can connect fans with a supply voltage of 12 V directly to the module. The connections FAN1, FAN2 and FAN3 have a speed monitoring function. The connected fan must supply a corresponding tachometer signal if this is to be used.

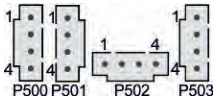


Fig. 5: FAN 1-4 connector

Pin assignment of fan P500 - P503

Pin assignment of fan P501			
P501	**Pin**	**Name**	**Description**
	1	FANON2	Fan 2 switched to ground
	2	12 V	12 V
	3	FANCTRL2	Fan 2 monitoring
	4	PWM2	Fan 2 power management

Pin assignment of fan P500			
P500	**Pin**	**Name**	**Description**
	1	FANON11	Fan 1 switched to ground
	2	12 V	12 V
	3	FANCTRL1	Fan 1 monitoring
	4	PWM1	Fan 1 power management

Pin assignment of fan P502			
P502	**Pin**	**Name**	**Description**
	1	FANON3	Fan 3 switched to ground
	2	12 V	12 V
	3	FANCTRL3	Fan 3 monitoring
	4	PWM3	Fan 3 power management

Pin assignment of fan P503			
P503	**Pin**	**Name**	**Description**
	1	FANON3	Fan 4 switched to ground, connected to fan 3
	2	12 V	12 V
	3	N/C	
	4	N/C	

Pin assignment with FAN4

FAN4 is connected to FAN3 via pin 1. Pins 3 and 4 not connected (N/C).

5.5 CD-In (P1200)

In addition to the external jack sockets, there is also an internal 4-pin housing connector (Foxconn HF1104E-P1) on the CB1067 board via which the other audio signals can be made available.

Fig. 6: CD-In plug

CD-In pin assignment		
Pin	**Name**	**Description**
1	CD_L	CD left channel
2	CD_GND	CD ground
3	CD_GND	CD ground
4	CD_R	CD right channel

5.6 Battery (BT1800/P1801)

The board is supplied with a CR2032 battery holder including a 3 V battery, but can also be connected to an external battery via a two-pin housing connector in order to continue to supply power to the integrated clock in the event of failure of the supply voltage.

Fig. 7: Battery connector

Pin assignment RTC battery connector		
Pin	**Name**	**Description**
1	BATT	3.3 V battery voltage
2	GND	Ground

5.7 Clear CMOS (J1800/1801)

If the board no longer boots up or the BIOS setup can no longer be called, then you can reset the settings stored in the CMOS with the "Clear CMOS" jumpers. To do this you must switch the computer off and first remove jumper 1 and then jumper 2 from their normal positions (contacts 1 and 2 closed) and plug them into the position "contacts 2 and 3 closed". After a few seconds, place the jumpers back in their normal positions again. Subsequently, the board boots up with the default settings as delivered ex factory.

Fig. 8: Clear CMOS jumpers

NOTE

Jumper settings

Prevent the system from entering an undefined state and make sure that the short-circuiting of the **Clear CMOS 1 jumper (J1800)** takes place **BEFORE** and **only together** with the setting of the **Clear CMOS 2 jumper (J1801)**.

Please also remember that resetting the CMOS will delete all settings made in the BIOS setup and thus also the time and date saved there, therefore the clock has to be set again afterwards.

5.8 Memory SO-DIMM260 (U600/700 and U601/701)

On the CB1067 board there are four SO-DIMM260 memory slots for DDR4-2666 RAM. For technical and mechanical reasons, it is possible that certain memory modules cannot be used. Information regarding the recommended memory modules can be obtained from your distributor.

With four slots, a memory extension up to 128 GB is possible with currently available modules.

All timing parameters for the different makes and versions are automatically set by the BIOS.

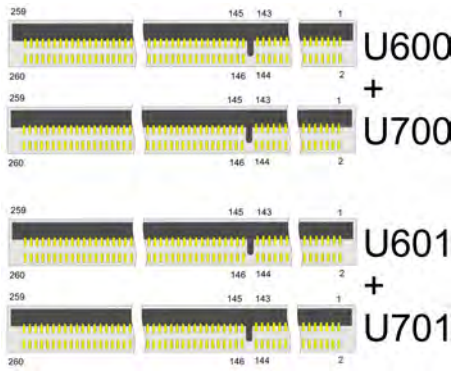


Fig. 9: SO-DIMM260 connector

Pin assignment SO-DIMM260					
Description	**Name**	**Pin**		**Name**	**Description**
Ground	GND	1	2	GND	Ground
Data line 5	DQ5	3	4	DQ4	Data line 4
Ground	GND	5	6	GND	Ground
Data line 1	DQ1	7	8	DQ0	Data line 0
Ground	GND	9	10	GND	Ground
Data strobe 0 -	DQS0#	11	12	DQM0	Data Mask 0
Data strobe 0 +	DQS0	13	14	GND	Ground
Ground	GND	15	16	DQ6	Data line 6
Data line 7	DQ7	17	18	GND	Ground
Ground	GND	19	20	DQ2	Data line 2
Data line 3	DQ3	21	22	GND	Ground
Ground	GND	23	24	DQ12	Data line 12
Data line 13	DQ13	25	26	GND	Ground
Ground	GND	27	28	DQ8	Data line 8
Data line 9	DQ9	29	30	GND	Ground
Ground	GND	31	32	DQS1#	Data strobe 1 -
Data Mask 1	DQM1	33	34	DQS1	Data strobe 1 +
Ground	GND	35	36	GND	Ground
Data line 15	DQ15	37	38	DQ14	Data line 14
Ground	GND	39	40	GND	Ground
Data line 10	DQ10	41	42	DQ11	Data line 11
Ground	GND	43	44	GND	Ground
Data line 21	DQ21	45	46	DQ20	Data line 20
Ground	GND	47	48	GND	Ground
Data line 17	DQ17	49	50	DQ16	Data line 16
Ground	GND	51	52	GND	Ground
Data strobe 2 -	DQS2#	53	54	DQM2	Data Mask 2
Data strobe 2 +	DQS2	55	56	GND	Ground
Ground	GND	57	58	DQ22	Data line 22
Data line 23	DQ23	59	60	GND	Ground
Ground	GND	61	62	DQ18	Data line 18
Data line 19	DQ19	63	64	GND	Ground
Ground	GND	65	66	DQ28	Data line 28
Data line 29	DQ29	67	68	GND	Ground
Ground	GND	69	70	DQ24	Data line 24
Data line 25	DQ25	71	72	GND	Ground
Ground	GND	73	74	DQS3#	Data strobe 3 -
Data Mask 3	DQM3	75	76	DQS3	Data strobe 3 +
Ground	GND	77	78	GND	Ground
Data line 30	DQ30	79	80	DQ31	Data line 31
Ground	GND	81	82	GND	Ground
Data line 26	DQ26	83	84	DQ27	Data line 27
Ground	GND	85	86	GND	Ground
Not connected	CB5 / NC	87	88	CB4 / NC	Not connected
Ground	GND	89	90	GND	Ground
Not connected	CB1 / NC	91	92	CB0 / NC	Not connected
Ground	GND	93	94	GND	Ground

Pin assignment SO-DIMM260					
Description	**Name**	**Pin**		**Name**	**Description**
Data strobe 8 -	DQS8#	95	96	DQM8	Data Mask 8
Data strobe 8 +	DQS8	97	98	GND	Ground
Ground	GND	99	100	CB6 / NC	Not connected
Not connected	CB2 / NC	101	102	GND	Ground
Ground	GND	103	104	CB4 / NC	Not connected
Not connected	CB3 / NC	105	106	GND	Ground
Ground	GND	107	108	RESET_n	Reset
Clock Enable 0	CKE0	109	110	CKE1	Clock Enable 1
1.2 V supply voltage	M_VDD	111	112	M_VDD	1.2 V supply voltage
Bank Group Input 1	BG1	113	114	ACT_n	Activation Command Input
Bank Group Input 0	BG0	115	116	ALERT_n	Alert
1.2 V supply voltage	M_VDD	117	118	M_VDD	1.2 V supply voltage
Address line 12	A12	119	120	A11	Address line 11
Address line 9	A9	121	122	A7	Address line 7
1.2 V supply voltage	M_VDD	123	124	VCC	1.2 V supply voltage
Address line 8	A8	125	126	A5	Address line 5
Address line 6	A6	127	128	A4	Address line 4
1.2 V supply voltage	M_VDD	129	130	M_VDD	1.2 V supply voltage
Address line 3	A3	131	132	A2	Address line 2
Address line 1	A1	133	134	EVENT_n	Event
1.2 V supply voltage	M_VDD	135	136	M_VDD	1.2 V supply voltage
Clock Signal 0 +	CK0_t	137	138	CK1_t	Clock 1+
Clock Signal 0 -	CK0_c	139	140	CK1_c	Clock 1 -
1.2 V supply voltage	M_VDD	141	142	M_VDD	1.2 V supply voltage
Even parity check	PAR	143	144	A0	Address line 0
SDRAM Bank 2	BA1	145	146	A10/AP	Address line10/ auto precharge
1.2 V supply voltage	M_VDD	147	148	M_VDD	1.2 V supply voltage
Chip Select 0	CS0_n	149	150	BA0	Bank Address 0
Address line 14/ Write Enable	A14/WE_n	151	152	A16/RAS_n	Address line 16/Row Address Strobe
1.2 V supply voltage	M_VDD	153	154	M_VDD	1.2 V supply voltage
On Die Termination 0	ODT0	155	156	A15/CAS_n	Address line 15/Column Address Strobe
Chip Select 1	CS1_n	157	158	A13	Address line 13
1.2 V supply voltage	M_VDD	159	160	M_VDD	1.2 V supply voltage
On Die Termination 1	ODT1	161	162	S2 / NC	Not connected
1.2 V supply voltage	M_VDD	163	164	VREFCA	Reference voltage
Not connected	S3 / NC	165	166	SA2	SPD Address 2
Ground	GND	167	168	GND	Ground
Data line 37	DQ37	169	170	DQ36	Data line 36
Ground	GND	171	172	GND	Ground
Data line 33	DQ33	173	174	DQ32	Data line 32
Ground	GND	175	176	GND	Ground
Data strobe 4 -	DQS4#	177	178	DQM4	Data Mask
Data strobe 4 +	DQS4	179	180	GND	Ground
Ground	GND	181	182	DQ39	Data line 39

Pin assignment SO-DIMM260					
Description	**Name**	**Pin**		**Name**	**Description**
Data line 38	DQ38	183	184	GND	Ground
Ground	GND	185	186	DQ35	Data line 35
Data line 34	DQ34	187	188	GND	Ground
Ground	GND	189	190	DQ45	Data line 45
Data line 44	DQ44	191	192	GND	Ground
Ground	GND	193	194	DQ41	Data line 41
Data line 40	DQ40	195	196	GND	Ground
Ground	GND	197	198	DQS5#	Data strobe 5 -
Data Mask 5	DQM5	199	200	DQS5	Data strobe 5 +
Ground	GND	201	202	GND	Ground
Data line 46	DQ46	203	204	DQ47	Data line 47
Ground	GND	205	206	GND	Ground
Data line 42	DQ42	207	208	DQ43	Data line 43
Ground	GND	209	210	GND	Ground
Data line 52	DQ52	211	212	DQ53	Data line 53
Ground	GND	213	214	GND	Ground
Data line 49	DQ49	215	216	DQ48	Data line 48
Ground	GND	217	218	GND	Ground
Data strobe 6 -	DQS6#	219	220	DQM6	Data Mask
Data strobe 6 +	DQS6	221	222	GND	Ground
Ground	GND	223	224	DQ54	Data line 54
Data line 55	DQ55	225	226	GND	Ground
Ground	GND	227	228	DQ50	Data line 50
Data line 51	DQ51	229	230	GND	Ground
Ground	GND	231	232	DQ60	Data line 60
Data line 61	DQ61	233	234	GND	Ground
Ground	GND	235	236	DQ57	Data line 57
Data line 56	DQ56	237	238	GND	Ground
Ground	GND	239	240	DQS7#	Data strobe 7 -
Data Mask 7	DQM7	241	242	DQS7	Data strobe 7 +
Ground	GND	243	244	GND	Ground
Data line 62	DQ62	245	246	DQ63	Data line 63
Ground	GND	247	248	GND	Ground
Data line 58	DQ58	249	250	DQ59	Data line 59
Ground	GND	251	252	GND	Ground
SMBus Clock	SCL	253	254	SDA	SMBus Data
I²C power for SPD EEProm	VCCSPD 3.3 V	255	256	SA0	SPD Address 0
DRAM Activating Power	VPP	257	258	M_VTT	Termination voltage
DRAM Activating Power	VPP	259	260	SA1	SPD Address 1

5.9 Power supply (P1800 and P1802)

The connection for the power supply is implemented as a 2x12-pin standard ATX plug ("ATX24"). This is supplemented by a 2x4-pin housing connector of its own, via which the CORE-IN voltage must be provided.

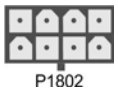


Fig. 10: 2x4-pin MiniFit connector - new

Pin assignment of 2x4-pin MiniFit connector					
Description	**Name**	**Pin**		**Name**	**Description**
Ground	GND	1	5	COREIN	12 V supply voltage
Ground	GND	2	6	COREIN	12 V supply voltage
Ground	GND	3	7	COREIN	12 V supply voltage
Ground	GND	4	8	COREIN	12 V supply voltage

Fig. 11: 2x12-pin ATX power connector

Pin assignment of 2x12-pin ATX power connector					
Description	**Name**	**Pin**		**Name**	**Description**
3.3 V supply voltage	3.3 V	1	13	3.3 V	3.3 V supply voltage
3.3 V supply voltage	3.3 V	2	14	-12 V	–12 V supply voltage
Ground	GND	3	15	GND	Ground
5 V supply voltage	VCC	4	16	PS_ON	On/Off signal
Ground	GND	5	17	GND	Ground
5 V supply voltage	VCC	6	18	GND	Ground
Ground	GND	7	19	GND	Ground
ATX Power good	PWR_ON	8	20	-5 V	–5 V supply voltage
Standby 5 V	S VCC	9	21	VCC	5 V supply voltage
12 V supply voltage	12 V	10	22	VCC	5 V supply voltage
12 V supply voltage	12 V	11	23	VCC	5 V supply voltage
3.3 V supply voltage	3.3 V	12	24	GND	Ground

5.10 SATA (P504 - P509)

Six SATA connectors are available for the connection of SATA devices. All SATA channels support the speed modes 1.5 Gbit/s, 3 Gbit/s and 6 Gbit/s.

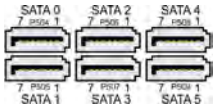


Fig. 12: SATA connector

Pin assignment of SATA connector		
Pin	**Name**	**Description**
1	GND	Ground
2	SATATX	SATA Transmit +
3	SATATX#	SATA Transmit -
4	GND	Ground
5	SATARX#	SATA Receive -
6	SATARX	SATA Receive +
7	GND	Ground

5.11 Connector System 1 (P1603)

The board has a 2x13-pin standard pin contact strip for insulation displacement contact technology with a spacing of 2.54 mm, via which the signals for power button, speaker, reset and various status LEDs are provided. This connector is coded for Beckhoff.

Fig. 13: System connectors

Pin assignment of connector system 1					
Description	**Name**	**Pin**		**Name**	**Description**
On/Suspend button	PWRBTN#	A1	B1	GND	Ground
Ground	S VCC	A2	B2	N/C	Not connected
Not available	N/C	A3	B3	PWLED#	Power LED
Ground	GND	A4	B4	N/C	Not connected
5 V supply voltage	VCC	A5	B5	PWLED	3.3 V supply voltage
Hard disk LED	HDLED#	A6	B6	N/C	Not available
5 V supply voltage	VCC	A7	B7	VCC	5 V supply voltage
Not available	N/C	A8	B8	GND	Ground
Not connected	N/C	A9	B9	N/C	Not connected
Ground	GND	A10	B10	BEEP	Speaker
Not connected	N/C	A11	B11	N/C	Not available
Not connected	N/C	A12	B12	GND	Ground
5 V supply voltage	VCC	A13	B13	RESET#	Reset

Connector system 2

The board is prepared for a further 2x9-pin system connector (P1605) and can be fitted with it.

5.12 GPIO (P800)

The board has a general purpose input/output interface that is fed out via a 2x10-pin connector. By programming the associated chip (Super-IO) accordingly, I/O functions can be created here in a very flexible manner. Ask your distributor about appropriate software support.

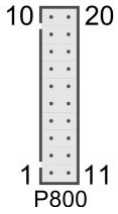


Fig. 14: GPIO connector

Pin assignment of GPIO connector					
Description	**Name**	**Pin**		**Name**	**Description**
5 V supply voltage	VCC	1	11	VCC	5 V supply voltage
GP Input/Output 0	GPIO0	2	12	N/C	Not connected
GP Input/Output 1	GPIO1	3	13	N/C	Not connected
GP Input/Output 2	GPIO2	4	14	N/C	Not connected
GP Input/Output 3	GPIO3	5	15	N/C	Not connected
GP Input/Output 4	GPIO4	6	16	N/C	Not connected
GP Input/Output 5	GPIO5	7	17	N/C	Not connected
GP Input/Output 6	GPIO6	8	18	N/C	Not connected
GP Input/Output 7	GPIO7	9	19	N/C	Not connected
Ground	GND	10	20	GND	Ground

5.13 SMB/I²C (P1600)

The module is capable of communicating with other switching elements via the SMBus or the I²C protocol. The connections for this are implemented in a 2x5-pin connector. The SMBus signals are processed by the chipset, the I²C signals by the SIO chip.

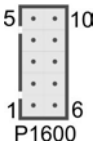
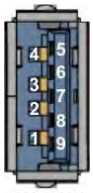


Fig. 15: SMB-I²C

Pin assignment of SMB/I²C connector					
Description	**Name**	**Pin**		**Name**	**Description**
3.3 V supply voltage	3.3 V	1	6	GND	Ground
SMBus Clock	SMBCLK	2	7	SMBDAT	SMBus Data
SMBus Alarm	SMBALERT#	3	8	S VCC	Standby supply 5 V
I²C-Bus Clock	I2CLK	4	9	I2DAT	I²C-Bus Data
5 V supply voltage	VCC	5	10	GND	Ground

5.14 USB 3.0 type A (P1712)

USB3 channel 5 is provided via an internal USB interface.



P1712

Fig. 16: USB 3.0 type A

Pin assignment of internal USB 3.0 connector		
Pin	**Name**	**Description**
1	VCC	5 V for USB
2	USB#	Minus data channel USB
3	USB	Plus data channel USB
4	GND1	Ground
5	StdA_SSRX-	SuperSpeed Receiver -
6	StdA_SSRX+	SuperSpeed Receiver +
7	GND2	Ground
8	StdA_SSTX-	SuperSpeed Transmitter -
9	StdA_SSTX+	SuperSpeed Transmitter +

5.15 USB 2.0 (P1708 - 1711)

USB channels 7 - 14 are provided via four 2x5-pin connectors.

The USB channels support the USB specification 2.0.

All necessary settings for USB can be made by the BIOS. Note that the "USB mouse and keyboard" function in the BIOS setup is only required if the operating system does not offer USB support. This function should not be selected for settings in the setup and for booting Windows with a USB mouse and keyboard connected, because this would lead to considerable performance limitations.

The individual USB interfaces can supply a current of up to 500 mA and are electronically protected.

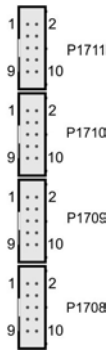


Fig. 17: USB 2.0 internal

Pin assignment of internal USB 2.0 connector					
Description	**Name**	**Pin**		**Name**	**Description**
5 V for USBx	VCC	1	2	VCC	5 V for USBy
Minus data channel USBx	USBx-	3	4	USBy-	Minus data channel USBy
Plus data channel USBx	USBx+	5	6	USBy+	Plus data channel USBy
Ground	GND	7	8	GND	Ground
Not connected	N/C	9	10	N/C	Not connected

5.16 Serial interfaces COM2/3/4 (P1702/P1704/P1706)

The three other serial interfaces available on the board – COM2/3/4 to are each fed out in the form of a 2x5-pin connector. The signals correspond to the RS232 standard.

The port address and the interrupt used are set with the help of the BIOS setup.

2x5-pin connector:

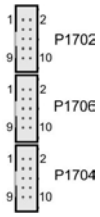


Fig. 18: COM 2/3/4

Pin assignment of COM connector					
Description	**Name**	**Pin**		**Name**	**Description**
Data Carrier Detect	DCD	1	2	DSR	Data Set Ready
Receive Data	RXD	3	4	RTS	Request to Send
Transmit Data	TXD	5	6	CTS	Clear to Send
Data Terminal Ready	DTR	7	8	RI	Ring Indicator
Ground	GND	9	10	VCC	5 V supply voltage

5.17 PCI interfaces (P1300 and P1301)

The CB1067 board has two standard PCI slots for expansion cards.

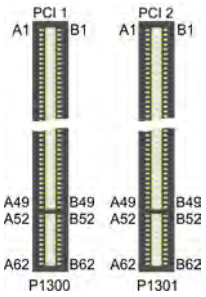


Fig. 19: PCI connector

NOTE

Observe pin assignment

In the pin assignment table below, note that for certain signals there are necessary differences between the different PCI connectors on the board. This applies to the test data signals (A4, B4), the interrupt signals (A6, A7, B7, B8), the clock signal (B16), the grant signal (A17), the request signal (B18) and the ID select signal (A26).

Pin assignment of PCI connector					
Description	**Name**	**Pin**		**Name**	**Description**
Test Logic Reset	TRST#	A1	B1	-12 V	–12 V supply voltage
12 V supply voltage	12 V	A2	B2	TCK	Test Clock
Test Mode Select	TMS	A3	B3	GND	Ground
Test Data Input	TDI	A4	B4	TDO	Test Data Output
5 V supply voltage	VCC	A5	B5	VCC	5 V supply voltage
Interrupt A	INTA#	A6	B6	VCC	5 V supply voltage
Interrupt C	INTC#	A7	B7	INTB#	Interrupt B
5 V supply voltage	VCC	A8	B8	INTD#	Interrupt D
Not connected	N/C	A9	B9	GND	Ground
5 V supply voltage	VCC	A10	B10	N/C	Not connected
Reserved	N/C	A11	B11	GND	Ground
Ground	GND	A12	B12	GND	Ground
Ground	GND	A13	B13	GND	Ground
3.3 V supply voltage	3.3 VAux	A14	B14	N/C	Not connected
PCI Reset	PRST#	A15	B15	GND	Ground
5 V supply voltage	VCC	A16	B16	PCLK	Clock
Grant PCI Use	GNT#	A17	B17	GND	Ground
Ground	GND	A18	B18	REQ#	Request
Power Management Event	PME#	A19	B19	VCC	5 V supply voltage
Address/Data 30	AD30	A20	B20	AD31	Address/Data 31
3.3 V supply voltage	3.3 V	A21	B21	AD29	Address/Data 29
Address/Data 28	AD28	A22	B22	GND	Ground
Address/Data 26	AD26	A23	B23	AD27	Address/Data 27
Ground	GND	A24	B24	AD25	Address/Data 25
Address/Data 24	AD24	A25	B25	3.3 V	3.3 V supply voltage
Init Device Select	IDSEL	A26	B26	CBE3#	Command Byte Enable 3
3.3 V supply voltage	3.3 V	A27	B27	AD23	Address/Data 23
Address/Data 22	AD22	A28	B28	GND	Ground
Address/Data 20	AD20	A29	B29	AD21	Address/Data 21
Ground	GND	A30	B30	AD19	Address/Data 19
Address/Data 18	AD18	A31	B31	3.3 V	3.3 V supply voltage
Address/Data 16	AD16	A32	B32	AD17	Address/Data 17
3.3 V supply voltage	3.3 V	A33	B33	CBE2#	Command, Byte Enable 2
Cycle Frame	FRAME#	A34	B34	GND	Ground
Ground	GND	A35	B35	IRDY#	Initiator Ready
Target Ready	TRDY#	A36	B36	3.3 V	3.3 V supply voltage
Ground	GND	A37	B37	DEVSEL#	Device Select
Stop Request by Target	STOP#	A38	B38	GND	Ground
3.3 V supply voltage	3.3 V	A39	B39	PLOCK#	Lock Bus
SMBus Clock PCI	SMBCLK	A40	B40	PERR#	Parity error
SMBus Data PCI	SMBDAT	A41	B41	3.3 V	3.3 V supply voltage
Ground	GND	A42	B42	SERR#	System Error
Parity	PAR	A43	B43	3.3 V	3.3 V supply voltage
Address/Data 15	AD15	A44	B44	CBE1#	Command, Byte Enable 1
3.3 V supply voltage	3.3 V	A45	B45	AD14	Address/Data 14
Address/Data 13	AD13	A46	B46	GND	Ground
Address/Data 11	AD11	A47	B47	AD12	Address/Data 12

Pin assignment of PCI connector					
Description	**Name**	**Pin**		**Name**	**Description**
Ground	GND	A48	B48	AD10	Address/Data 10
Address/Data 9	AD9	A49	B49	GND	Ground
Coded	N/C	A50	B50	N/C	Coded
Coded	N/C	A51	B51	N/C	Coded
Command, Byte Enable 0	CBE0#	A52	B52	AD8	Address/Data 8
3.3 V supply voltage	3.3 V	A53	B53	AD7	Address/Data 7
Address/Data 6	AD6	A54	B54	3.3 V	3.3 V supply voltage
Address/Data 4	AD4	A55	B55	AD5	Address/Data 5
Ground	GND	A56	B56	AD3	Address/Data 3
Address/Data 2	AD2	A57	B57	GND	Ground
Address/Data 0	AD0	A58	B58	AD1	Address/Data 1
5 V supply voltage	VCC	A59	B59	VCC	5 V supply voltage
5 V supply voltage	REQ64	A60	B60	VCC	5 V supply voltage
5 V supply voltage	VCC	A61	B61	VCC	5 V supply voltage
5 V supply voltage	VCC	A62	B62	VCC	5 V supply voltage

5.18 PCI-Express interfaces x4 (P1305 and P1302)

Two PCI-Express x4 expansion card slots are available on the CB1067 board. x1 expansion cards can also be operated in these slots.

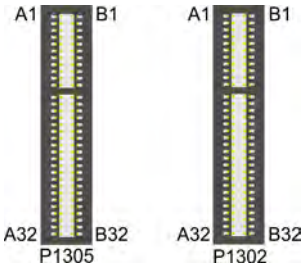


Fig. 20: PCIe x4 connector

Pin assignment of PCI-Express x4 connector					
Description	**Name**	**Pin**		**Name**	**Description**
Hot Plug Detect 1	PRSNT1#	A1	B1	12 V	12 V supply voltage
12 V supply voltage	12 V	A2	B2	12 V	12 V supply voltage
12 V supply voltage	12 V	A3	B3	RSVD	Not connected
Ground	GND	A4	B4	GND	Ground
Not connected	TCK	A5	B5	SMBCLK	SMBus Clock PCIe
Not connected	TDI	A6	B6	SMBDAT	SMBus Data PCIe
Not connected	TDO	A7	B7	GND	Ground
Not connected	TMS	A8	B8	3.3 V	3.3 V supply voltage
3.3 V supply voltage	3.3 V	A9	B9	TRST	Not connected
3.3 V supply voltage	3.3 V	A10	B10	S3.3V	Standby voltage 3.3 V
PCIe Reset	PERST#	A11	B11	PEWAKE#	Link Reactivation
Ground	GND	A12	B12	RSVD	Reserved
Reference Clock +	REFCLK	A13	B13	GND	Ground
Reference Clock -	REFCLK#	A14	B14	PET0	Transmit Lane 0 +
Ground	GND	A15	B15	PET0#	Transmit Lane 0 -
Receive Lane 0 +	PER0	A16	B16	GND	Ground
Receive Lane 0 -	PER0#	A17	B17	PRSNT2#	Hot Plug Detect 2
Ground	GND	A18	B18	GND	Ground
Not connected	RSVD	A19	B19	PET1	Transmit Lane 1 +
Ground	GND	A20	B20	PET1#	Transmit Lane 1 -
Receive Lane 1 +	PER1	A21	B21	GND	Ground
Receive Lane 1 -	PER1#	A22	B22	GND	Ground
Ground	GND	A23	B23	PET2	Transmit Lane 2 +
Ground	GND	A24	B24	PET2#	Transmit Lane 2 -
Receive Lane 2 +	PER2	A25	B25	GND	Ground
Receive Lane 2 -	PER2#	A26	B26	GND	Ground
Ground	GND	A27	B27	PET3	Transmit Lane 3 +
Ground	GND	A28	B28	PET3#	Transmit Lane 3 -
Receive Lane 3 +	PER3	A29	B29	GND	Ground
Receive Lane 3 -	PER3#	A30	B30	RSVD	Not connected
Ground	GND	A31	B31	PRSNT2#	Hot Plug Detect 2
Not connected	RSVD	A32	B32	GND	Ground

5.19 PCI-Express interface x16 (P1402)

A slot for PCI-Express x16 cards completes the range of available expansion options on the CB1067 board. This slot can be used for PCIe x16 graphics cards. An x1 or x4 expansion card can also be operated in this slot.

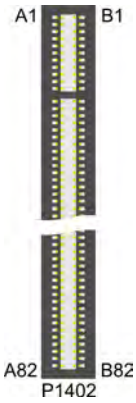


Fig. 21: PCIe x16 connector

Pin assignment of PCI-Express x16 connector					
Description	**Name**	**Pin**		**Name**	**Description**
Hot Plug Detect 1	PRSNT1#	A1	B1	12 V	12 V supply voltage
12 V supply voltage	12 V	A2	B2	12 V	12 V supply voltage
12 V supply voltage	12 V	A3	B3	RSVD	Reserved
Ground	GND	A4	B4	GND	Ground
Test Clock	TCK	A5	B5	SMBCLK	SMBus Clock PCIe
Not connected	TDI	A6	B6	SMBDAT	SMBus Data PCIe
Not connected	TDO	A7	B7	GND	Ground
Not connected	TMS	A8	B8	3.3 V	3.3 V supply voltage
3.3 V supply voltage	3.3 V	A9	B9	TRST	Not connected
3.3 V supply voltage	3.3 V	A10	B10	S3.3V	Standby voltage 3.3 V
PCIe Reset	PERST#	A11	B11	PEWAKE#	Link Reactivation
Ground	GND	A12	B12	RSVD	Not connected
Reference Clock +	REFCLK	A13	B13	GND	Ground
Reference Clock -	REFCLK#	A14	B14	PET0	Transmit Lane 0 +
Ground	GND	A15	B15	PET0#	Transmit Lane 0 -
Receive Lane 0 +	PER0	A16	B16	GND	Ground
Receive Lane 0 -	PER0#	A17	B17	PRSNT2#	Hot Plug Detect 2
Ground	GND	A18	B18	GND	Ground
Not connected	RSVD	A19	B19	PET1	Transmit Lane 1 +
Ground	GND	A20	B20	PET1#	Transmit Lane 1 -
Receive Lane 1 +	PER1	A21	B21	GND	Ground
Receive Lane 1 -	PER1#	A22	B22	GND	Ground
Ground	GND	A23	B23	PET2	Transmit Lane 2 +
Ground	GND	A24	B24	PET2#	Transmit Lane 2 -
Receive Lane 2 +	PER2	A25	B25	GND	Ground
Receive Lane 2 -	PER2#	A26	B26	GND	Ground
Ground	GND	A27	B27	PET3	Transmit Lane 3 +
Ground	GND	A28	B28	PET3#	Transmit Lane 3 -
Receive Lane 3 +	PER3	A29	B29	GND	Ground
Receive Lane 3 -	PER3#	A30	B30	RSVD	Not connected
Ground	GND	A31	B31	PRSNT2#	Hot Plug Detect 2
Not connected	RSVD	A32	B32	GND	Ground
Not connected	RSVD	A33	B33	PET4	Transmit Lane 4 +
Ground	GND	A34	B34	PET4#	Transmit Lane 4 -
Receive Lane 4 +	PER4	A35	B35	GND	Ground
Receive Lane 4 -	PER4#	A36	B36	GND	Ground
Ground	GND	A37	B37	PET5	Transmit Lane 5 +
Ground	GND	A38	B38	PET5#	Transmit Lane 5 -
Receive Lane 5 +	PER5	A39	B39	GND	Ground
Receive Lane 5 -	PER5#	A40	B40	GND	Ground
Ground	GND	A41	B41	PET6	Transmit Lane 6 +
Ground	GND	A42	B42	PET6#	Transmit Lane 6 -
Receive Lane 6 +	PER6	A43	B43	GND	Ground
Receive Lane 6 -	PER6#	A44	B44	GND	Ground
Ground	GND	A45	B45	PET7	Transmit Lane 7 +
Ground	GND	A46	B46	PET7#	Transmit Lane 7 -
Receive Lane 7 +	PER7	A47	B47	GND	Ground

Pin assignment of PCI-Express x16 connector					
Description	**Name**	**Pin**		**Name**	**Description**
Receive Lane 7 -	PER7#	A48	B48	PRSNT2#	Hot Plug Detect 2
Ground	GND	A49	B49	GND	Ground
Not connected	N/C	A50	B50	PET8	Transmit Lane 8 +
Ground	GND	A51	B51	PET8#	Transmit Lane 8 -
Receive Lane 8 +	PER8	A52	B52	GND	Ground
Receive Lane 8 -	PER8#	A53	B53	GND	Ground
Ground	GND	A54	B54	PET9	Transmit Lane 9 +
Ground	GND	A55	B55	PET9#	Transmit Lane 9 -
Receive Lane 9 +	PER9	A56	B56	GND	Ground
Receive Lane 9 -	PER9#	A57	B57	GND	Ground
Ground	GND	A58	B58	PET10	Transmit Lane 10 +
Ground	GND	A59	B59	PET10#	Transmit Lane 10 -
Receive Lane 10 +	PER10	A60	B60	GND	Ground
Receive Lane 10 -	PER10#	A61	B61	GND	Ground
Ground	GND	A62	B62	PET11	Transmit Lane 11 +
Ground	GND	A63	B63	PET11#	Transmit Lane 11 -
Receive Lane 11 +	PER11	A64	B64	GND	Ground
Receive Lane 11 -	PER11#	A65	B65	GND	Ground
Ground	GND	A66	B66	PET12	Transmit Lane 12 +
Ground	GND	A67	B67	PET12#	Transmit Lane 12 -
Receive Lane 12 +	PER12	A68	B68	GND	Ground
Receive Lane 12 -	PER12#	A69	B69	GND	Ground
Ground	GND	A70	B70	PET13	Transmit Lane 13 +
Ground	GND	A71	B71	PET13#	Transmit Lane 13 -
Receive Lane 13 +	PER13	A72	B72	GND	Ground
Receive Lane 13-	PER13#	A73	B73	GND	Ground
Ground	GND	A74	B74	PET14	Transmit Lane 14 +
Ground	GND	A75	B75	PET14#	Transmit Lane 14 -
Receive Lane 14 +	PER14	A76	B76	GND	Ground
Receive Lane 14 -	PER14#	A77	B77	GND	Ground
Ground	GND	A78	B78	PET15	Transmit Lane 15 +
Ground	GND	A79	B79	PET15#	Transmit Lane 15 -
Receive Lane 15 +	PER15	A80	B80	GND	Ground
Receive Lane 15 -	PER15#	A81	B81	DDAT-PRSNT	Reserved
Ground	GND	A82	B82	RSVD	Not connected

5.20 SPDIF connector (P1201)

An SPDIF connector is available for digital audio signals. This is internally connected to a 2x3-pin standard pin contact strip for insulation displacement contact technology with a spacing of 2.54 mm.

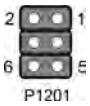


Fig. 22: SPDIF connector

Pin assignment of SPDIF connector					
Description	**Name**	**Pin**		**Name**	**Description**
Ground	GND	1	2	SPDIFO	SPDIF Out
3.3 V supply voltage	3.3 V	3	4	VCC	Supply voltage 5 V
Ground	GND	5	6	SPDIFI	SPDIF In

5.21 PCI-Express x1 (P1304 and P1303)

Two PCI-Express x1 expansion card slots are available on the CB10647 board.

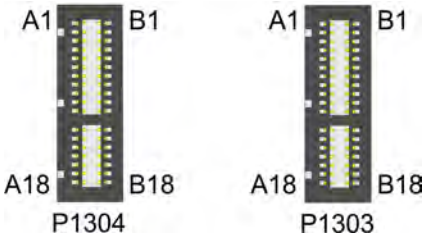


Fig. 23: PCIe x1 connector

NOTE

Observe pin assignment

In the pin assignment table below, note that for certain signals there are necessary differences between the different PCIe-x1 connectors on the board. This applies to the clock signals (A13, A14), the receive signals (A16, A17) and the transmit signals (B14, B15).

Pin assignment of PCI-Express x1 connector

Description	Name	Pin		Name	Description
Hot Plug Detect 1	PRSNT1#	A1	B1	12 V	12 V supply voltage
12 V supply voltage	12 V	A2	B2	12 V	12 V supply voltage
12 V supply voltage	12 V	A3	B3	RSVD	Not connected t
Ground	GND	A4	B4	GND	Ground
Not connected	TCK	A5	B5	SMBCLK	SMBus Clock PCIe
Not connected	TDI	A6	B6	SMBDAT	SMBus Data PCIe
Not connected	TDO	A7	B7	GND	Ground
Not connected	TMS	A8	B8	3.3 V	3.3 V supply voltage
3.3 V supply voltage	3.3 V	A9	B9	TRST	Reserved
3.3 V supply voltage	3.3 V	A10	B10	S3.3V	Standby voltage 3.3 V
PCIe Reset	PERST#	A11	B11	PEWAKE#	Link Reactivation
Ground	GND	A12	B12	RSVD	Not connected
Reference Clock +	REFCLK	A13	B13	GND	Ground
Reference Clock -	REFCLK#	A14	B14	PET0	Transmit Lane 0 +
Ground	GND	A15	B15	PET0#	Transmit Lane 0 -
Receive Lane 0 +	PER0	A16	B16	GND	Ground
Receive Lane 0 -	PER0#	A17	B17	PRSNT2#	Hot Plug Detect 2
Ground	GND	A18	B18	GND	Ground

5.22 Audio connections (P1602)

Connections for Line-In, Line-Out and microphone are fed out in the form of three jack sockets for 3.5 mm jack plugs.

Fig. 24: Audio connectors

5.23 LAN and USB 3.0 (P1401 and P1400)

For reasons of space, USB and LAN connectors are implemented in the form of two combination components, each providing two USB connectors and a LAN connector. In this way, four USB channels and two LAN ports are fed out with all board variants.

All USB channels support the 3.1 Gen2 specification.

All necessary settings for USB can be made by the BIOS. Note that the "USB Mouse and Keyboard" functionality of the BIOS setup is only required if the operating system does not provide USB support. Do not select this function for settings in the setup and for booting Windows with a connected USB mouse and keyboard, because this would result in significant performance limitations.

The individual USB interfaces can supply a current of up to 900 mA and are electronically protected.

Two Gigabit LAN ports are also available. In addition to 10BaseT and 100BaseT, 1000BaseT-compatible network components can also be connected to them. The required speed is selected automatically. Auto-Cross and Auto-Negotiate are supported as well as PXE. Controllers are i219 (PHY, LAN1) and i210 (MAC/PHY, LAN2).

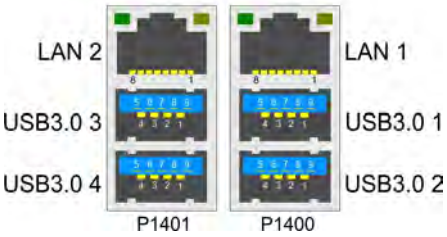


Fig. 25: LAN-USB3.0 connector

Real-time applications

The Ethernet port connected via PCIe is usually suitable for cycle times <= 1 ms and for distributed clock applications with EtherCAT.
The Ethernet port integrated in the chipset is usually suitable for real-time Ethernet applications with cycle times > 1 ms (without distributed clocks).

Pin assignment of LAN 10/100/1000		
Pin	**Name**	**Description**
1	LAN-0	LAN line 0 plus
2	LAN-0#	LAN line 0 minus
3	LAN-1	LAN line 1 plus
4	LAN-1#	LAN line 1 minus
5	LAN-2	LAN line 2 plus
6	LAN-2#	LAN line 2 minus
7	LAN-3	LAN line 3 plus
8	LAN-3#	LAN line 3 minus

Pin assignment of USB 3.1 connector		
Pin	**Name**	**Description**
1	VCC	5 V for USB
2	USB D#	Minus data channel USB
3	USB D	Plus data channel USB
4	GND1	Ground
5	SSRX -	SuperSpeed Receiver -
6	SSRX +	SuperSpeed Receiver +
7	GND2	Ground
8	SSTX -	SuperSpeed Transmitter -
9	SSTX +	SuperSpeed Transmitter +

5.24 DVI-D (P1500)

The CB1067 has two DVI-D connectors in a combination component (Foxconn QH11121-DBDF-4F). You can connect digital DVI or HDMI displays to both connectors. Analog signals are not available on this connector. The CPU graphics support a maximum of three independent displays.

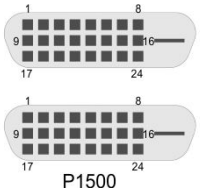


Fig. 26: DVI-D connector

Pin assignment of DVI-D		
Pin	**Name**	**Description**
1	TMDSDAT2#	DVI Data 2 -
2	TMDSDAT2	DVI Data 2 +
3	GND	Ground
4	N/C	Reserved
5	N/C	Reserved
6	DDC CLK	DDC Clock (DVI/VGA)
7	DDC DAT	DDC Data (DVI/VGA)
8	N/C	Reserved
9	TMDSDAT1#	DVI Data 1 -
10	TMDSDAT1	DVI Data 1 +
11	GND	Ground
12	N/C	Reserved
13	N/C	Reserved
14	VCC	5 V supply voltage
15	GND	Ground
16	HP_DETECT	Hot Plug Detect
17	TMDSDAT0#	DVI Data 0 -
18	TMDSDAT0	DVI Data 0 +
19	GND	Ground
20	N/C	Reserved
21	N/C	Reserved
22	GND	Ground
23	TMDS CLK	DVI-Clock
24	TMDS CLK#	DVI-Clock

5.25 Serial interface COM1 and DP/HDMI/DVI (P1700 and P1403)

The COM1 serial interface is fed out via a 9-pin standard DSUB connector. The signals correspond to the RS232 standard.

You can set the port address and the interrupt used with the help of the BIOS setup.

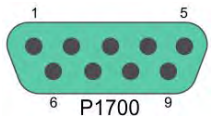


Fig. 27: COM1 connector

Pin assignment of COM1					
Description	**Name**	**Pin**		**Name**	**Description**
Data Carrier Detect	DCD#	1	6	DSR#	Data Set Ready
Receive Data	RXD	2	7	RTS#	Request to Send
Transmit Data	TXD	3	8	CTS#	Clear to Send
Data Terminal Ready	DTR#	4	9	RI#	Ring Indicator
Ground	GND	5			

A standard connector (Foxconn 3VC11203-D7AB-4H) is available for devices with a DisplayPort connector.

The interface additionally provides HDMI/DVI signals that can be used with aid of an adapter. Please consult your distributor with regard to a suitable adapter.

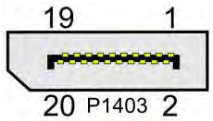


Fig. 28: DP connector

Pin assignment of DisplayPort					
Description	**Signal**	**Pin**		**Signal**	**Description**
Display Port Lane 0 +	L0	1	2	GND	Ground
Display Port Lane 0 -	L#0	3	4	L1	Display Port Lane 1 +
Ground	GND	5	6	L#1	Line 1 -
Display Port Lane 2 +	L2	7	8	GND	Ground
Display Port Lane 2 -	L#2	9	10	L3	Display Port Lane 3 +
Ground	GND	11	12	L#3	Display Port Lane 3 -
DP / HDMI	HDMI#	13	14	GND	Ground
Auxiliary plus	AUX	15	16	GND	Ground
Auxiliary minus	AUX#	17	18	HPD	Hot Plug Detect
Ground	GND	19	20	3.3 V	Supply voltage 3.3 V

6 BIOS settings

6.1 Using the setup

Within the individual setup pages the last saved settings can be restored can at any time with F2 ("Previous Values"). Use F3 ("Optimized Defaults") to load the factory defaults. Use F2/F3 to load the complete set of settings and F4 to save them ("Save & Exit").

A "►" sign in front of the menu item indicates that a submenu is available. Use the arrow keys to navigate between menu items. Use the Enter key to select menu items and call submenus or selection dialogs.

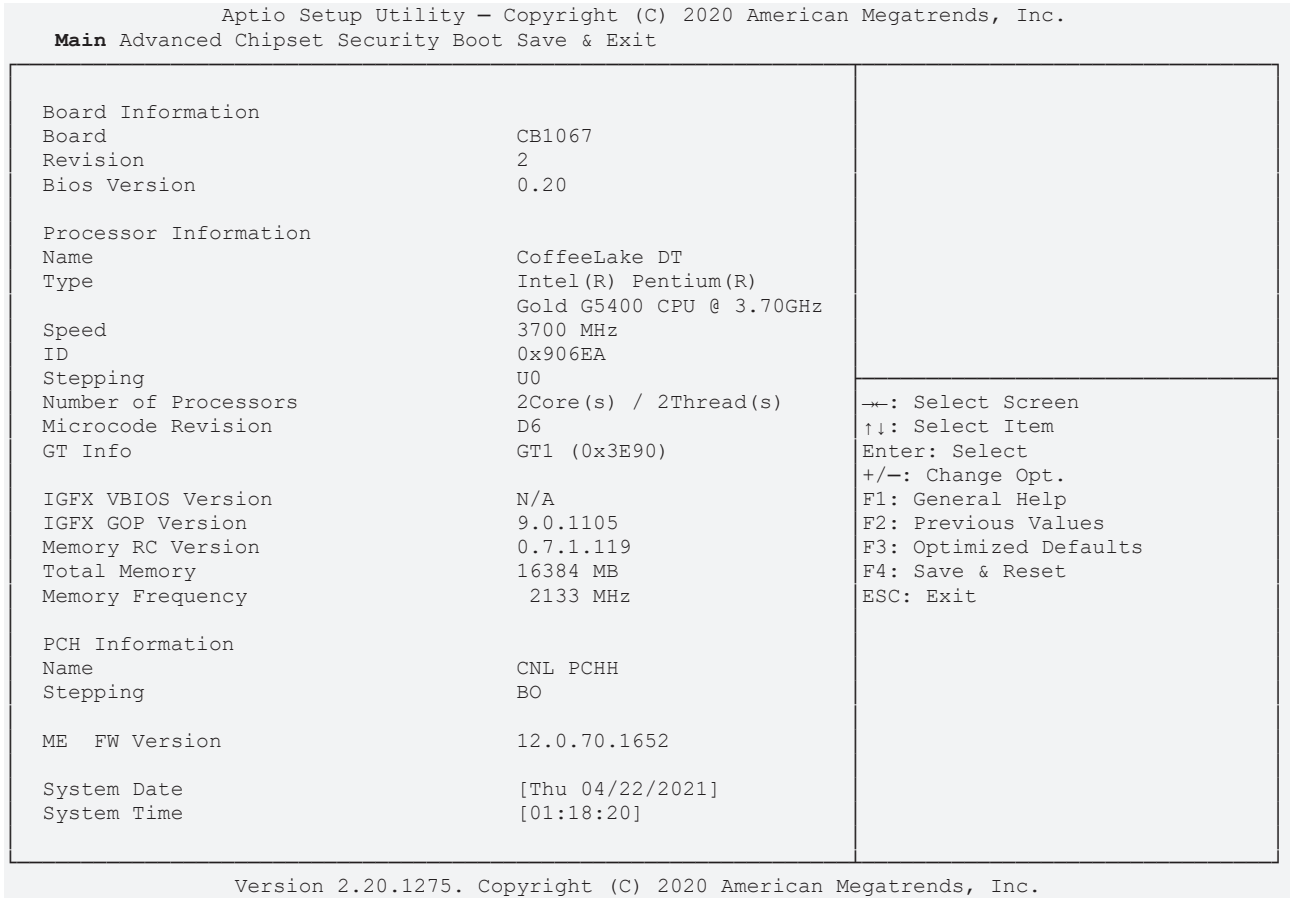
For each setup option a help text is displayed at the top right, which in many cases contains useful information about the option and permitted values, etc.

NOTE

Note on Setup Documentation

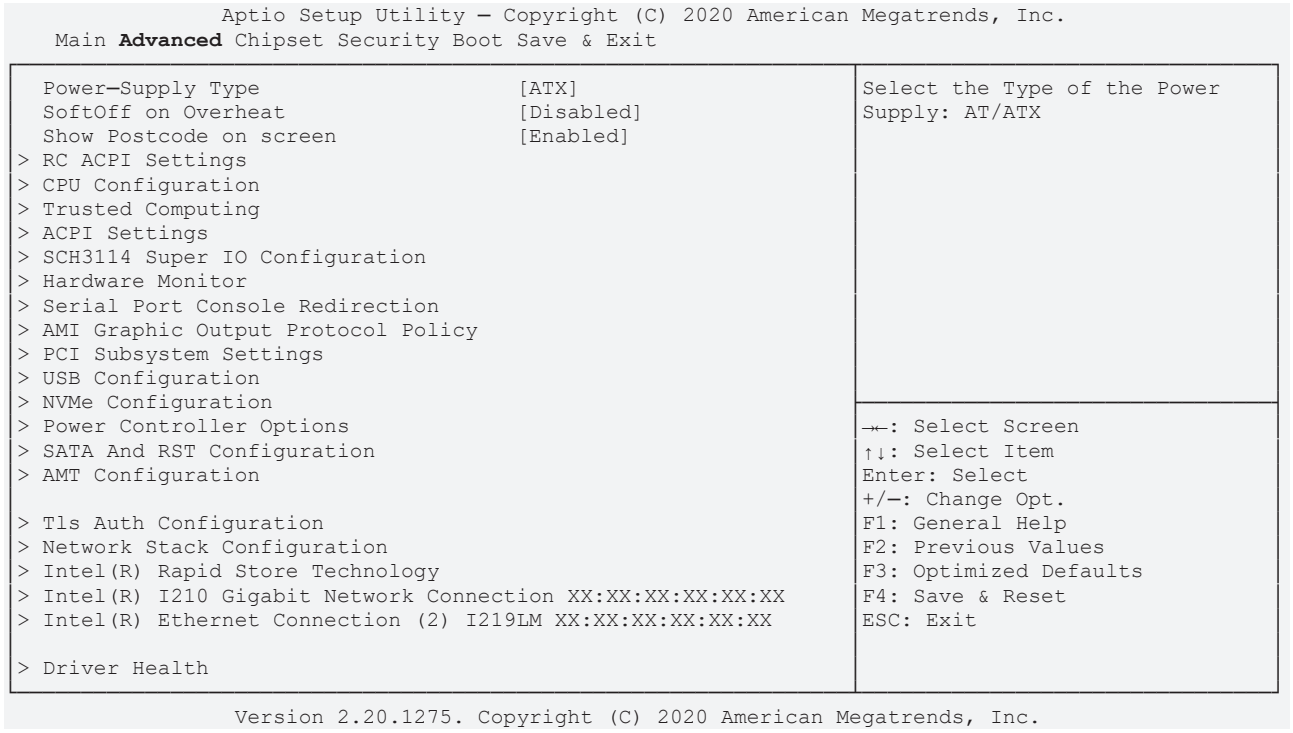
The BIOS is regularly updated so that the available setup options can change at any time without notice. This may result in differences between the options actually available and those described below. It should also be noted that the settings shown in the setup menus below are not necessarily the recommended or default settings. Which settings must be selected depends on the application scenario in which the board is operated.

6.2 Main


Aptio Setup Utility – Copyright (C) 2020 American Megatrends, Inc.
Main Advanced Chipset Security Boot Save & Exit
Board Information
Board CB1067
Revision 2
Bios Version 0.20
Processor Information
Name CoffeeLake DT
Type Intel(R) Pentium(R) Gold G5400 CPU @ 3.70GHz
Speed 3700 MHz
ID 0x906EA
Stepping U0
Number of Processors 2Core(s) / 2Thread(s)
Microcode Revision D6
GT Info GT1 (0x3E90)
IGFX VBIOS Version N/A
IGFX GOP Version 9.0.1105
Memory RC Version 0.7.1.119
Total Memory 16384 MB
Memory Frequency 2133 MHz
PCH Information
Name CNL PCHH
Stepping BO
ME FW Version 12.0.70.1652
System Date [Thu 04/22/2021]
System Time [01:18:20]
→←: Select Screen
↑↓: Select Item
Enter: Select
+/–: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Reset
ESC: Exit
Version 2.20.1275. Copyright (C) 2020 American Megatrends, Inc.

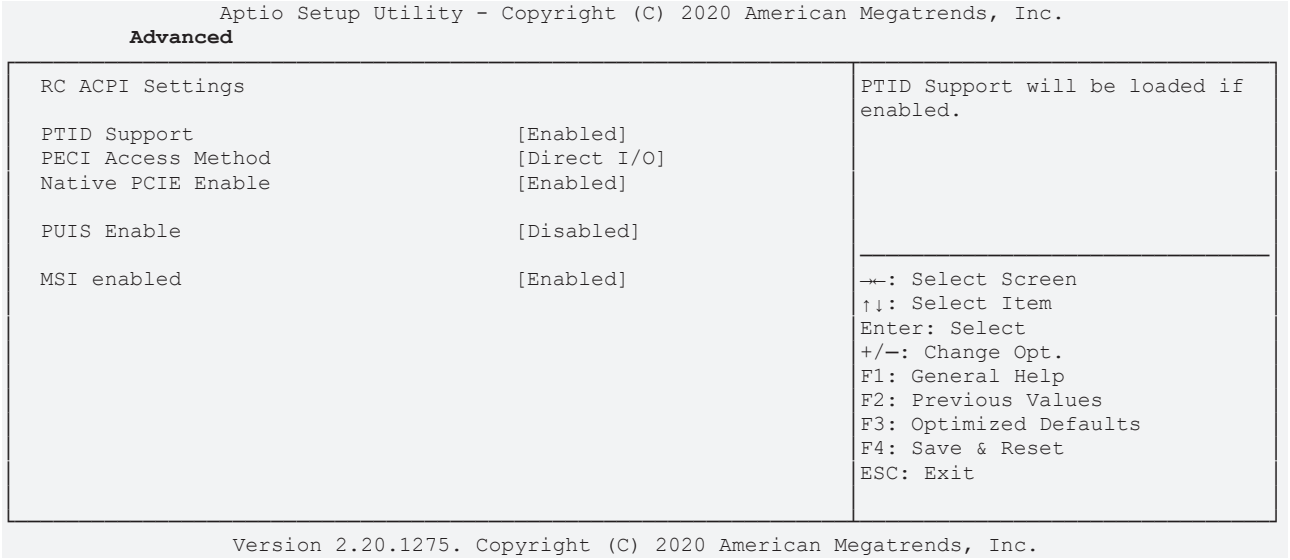
Bios entry	Option
Board information	
Board	None
Revision	None
Bios version	None
Processor Information	
Name	None
Type	None
Speed	None
ID	None
Stepping	None
Number of Processors	None
Microcode Revision	None
GT info	None
IGFX VBIOS Version	None
IGFX GOP Version	None
Memory RC Version	None
Total Memory	None
Memory Frequency	None
PCH information	
Name	None
Stepping	None
ME FW Version	None
System Date	Here you can change the system date.
System Time	Here you can change the system time.

6.3 Advanced


Aptio Setup Utility – Copyright (C) 2020 American Megatrends, Inc.
Main Advanced Chipset Security Boot Save & Exit
Power–Supply Type [ATX]
SoftOff on Overheat [Disabled]
Show Postcode on screen [Enabled]
> RC ACPI Settings
> CPU Configuration
> Trusted Computing
> ACPI Settings
> SCH3114 Super IO Configuration
> Hardware Monitor
> Serial Port Console Redirection
> AMI Graphic Output Protocol Policy
> PCI Subsystem Settings
> USB Configuration
> NVMe Configuration
> Power Controller Options
> SATA And RST Configuration
> AMT Configuration
> Tls Auth Configuration
> Network Stack Configuration
> Intel(R) Rapid Store Technology
> Intel(R) I210 Gigabit Network Connection XX:XX:XX:XX:XX:XX
> Intel(R) Ethernet Connection (2) I219LM XX:XX:XX:XX:XX:XX
> Driver Health
Select the Type of the Power Supply: AT/ATX
→←: Select Screen
↑↓: Select Item
Enter: Select
+/–: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Reset
ESC: Exit
Version 2.20.1275. Copyright (C) 2020 American Megatrends, Inc.

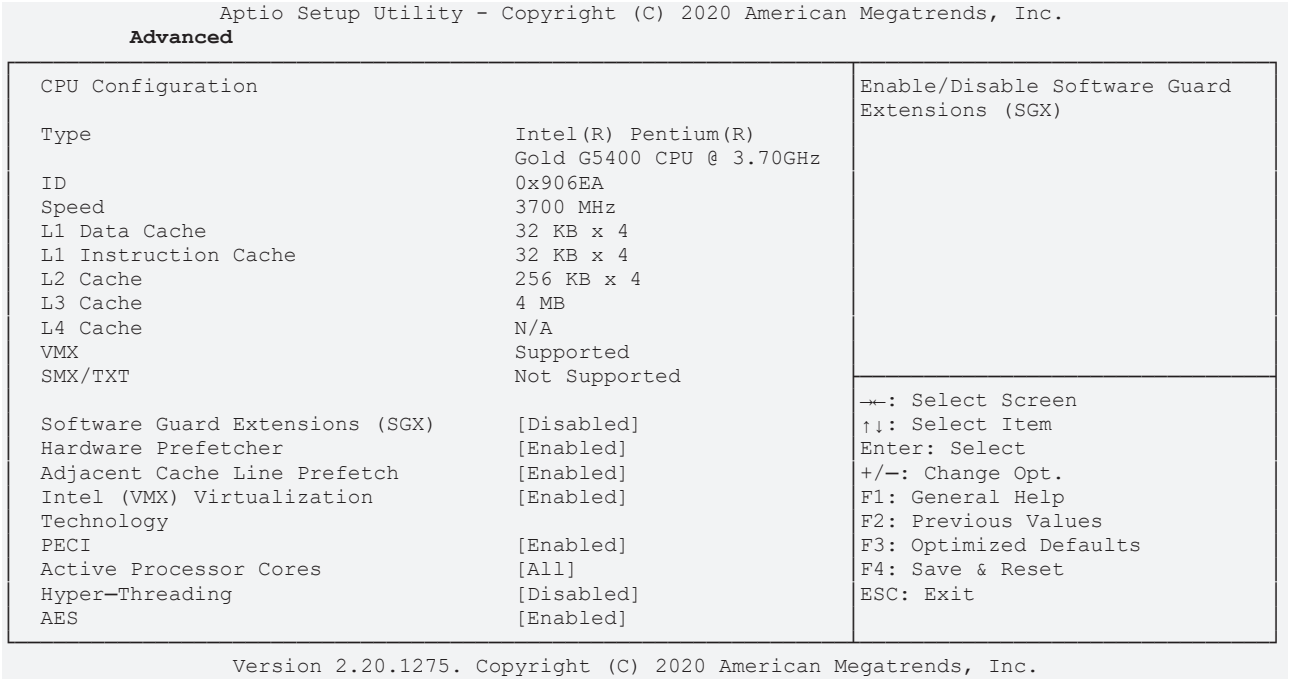
Bios entry	Option
Power-Supply Type	[ATX/AT]
SoftOff on Overheat	Disabled/Enabled/Enabled (Emulate PwrBtn)
RC ACPI Settings	Submenu see: RC ACPI settings [▶ 44]
CPU Configuration	Submenu see: CPU Configuration [▶ 45]
Trusted Computing	Submenu see: Trusted Computing [▶ 46]
ACPI Settings	Submenu see: ACPI Settings Enabled [▶ 46]
SCH3114 Super IO Configuration	Submenu see: SCH3114 Super IO Configuration [▶ 47]
Hardware Monitor	Submenu see: Hardware Monitor [▶ 52]
Serial Port Console Redirection	Submenu see: Serial Port Console Redirection [▶ 53]
AMI Graphic Output Protocol Policy	Submenu see: AMI Graphic Output Protocol Policy [▶ 58]
PCI Subsystem Settings	Submenu see: PCI Subsystem Settings [▶ 59]
USB Configuration	Submenu see: USB Configuration [▶ 61]
NVMe Configuration	Submenu see: NVMe Configuration [▶ 62]
Power Controller Options	Submenu see: Power Controller Options [▶ 63]
SATA And RST Configuration	Submenu see: SATA And RST Configuration [▶ 64]
AMT Configuration	Submenu see: AMT Configuration [▶ 66]
Tls Auth configuration	Submenu see: TLs Auth Configuration [▶ 70]
Network Stack Configuration	Submenu see: Network Stack Configuration [▶ 72], Network Stack Configuration enabled [▶ 73]
Intel® Rapid Store Technology	Submenu see: Intel Rapid Storage Technology [▶ 73]
Intel(R) I210 Gigabit Network Connection XX:XX:XX:XX:XX:XX	Submenu see: NIC Configuration [▶ 75]
Intel(R) Ethernet Connection (2) I219LM XX:XX:XX:XX:XX:XX	Submenu see: NIC Configuration [▶ 77]
Driver Health	Submenu see: Driver Health [▶ 78]

6.3.1 RC ACPI settings



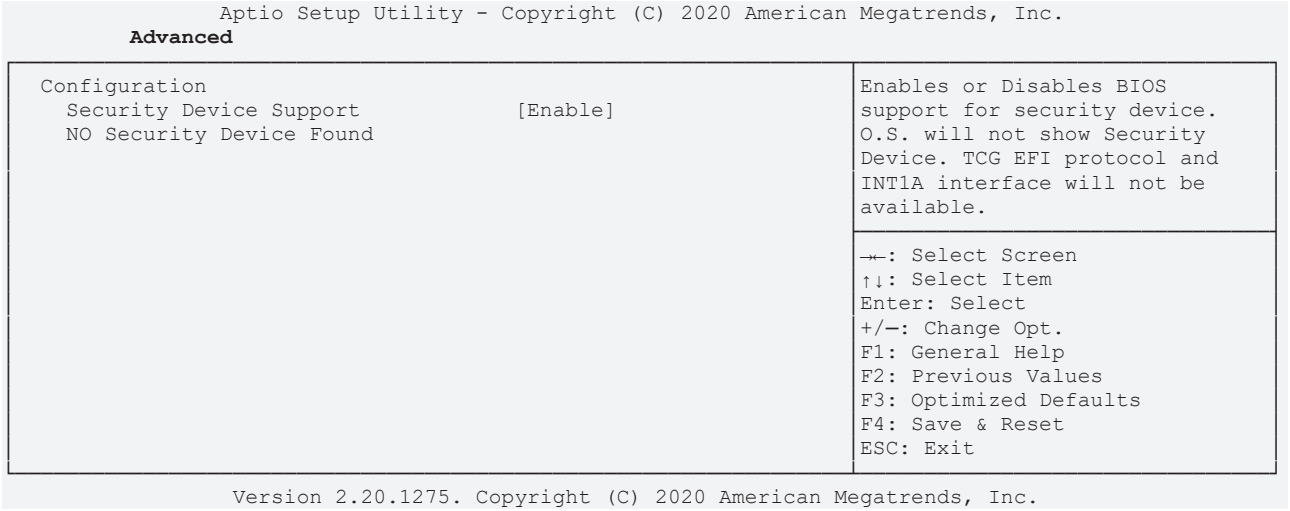
Bios entry	Options
RC ACPI settings	
PTID Support	Enabled/Disabled
PECI Access Method	Direct I/O
Native PCIE Enable	Enabled/Disabled
PUIS Enable	None
MSI enabled	Enabled/Disabled

6.3.2 CPU Configuration



Bios entry	Options
CPU Configuration	
Type	None
ID	None
Speed	None
L1 Data Cache	None
L1 instruction cache	None
L2 Cache	None
L3 Cache	None
L4 cache	None
VMX	None
SMX/TXT	None
Software Guard Extensions (SGX)	Disabled/Enabled/Software Controlled
Hardware prefetcher	Enabled/Disabled
Adjacent Cache Line Prefetch	Enabled/Disabled
Intel (VMX) Virtualization Technology	Enabled/Disabled
PECI	Enabled/Disabled
Active Processor Cores	All/1
Hyper-Threading	Disabled/Enabled
AES	Enabled/Disabled

6.3.3 Trusted Computing

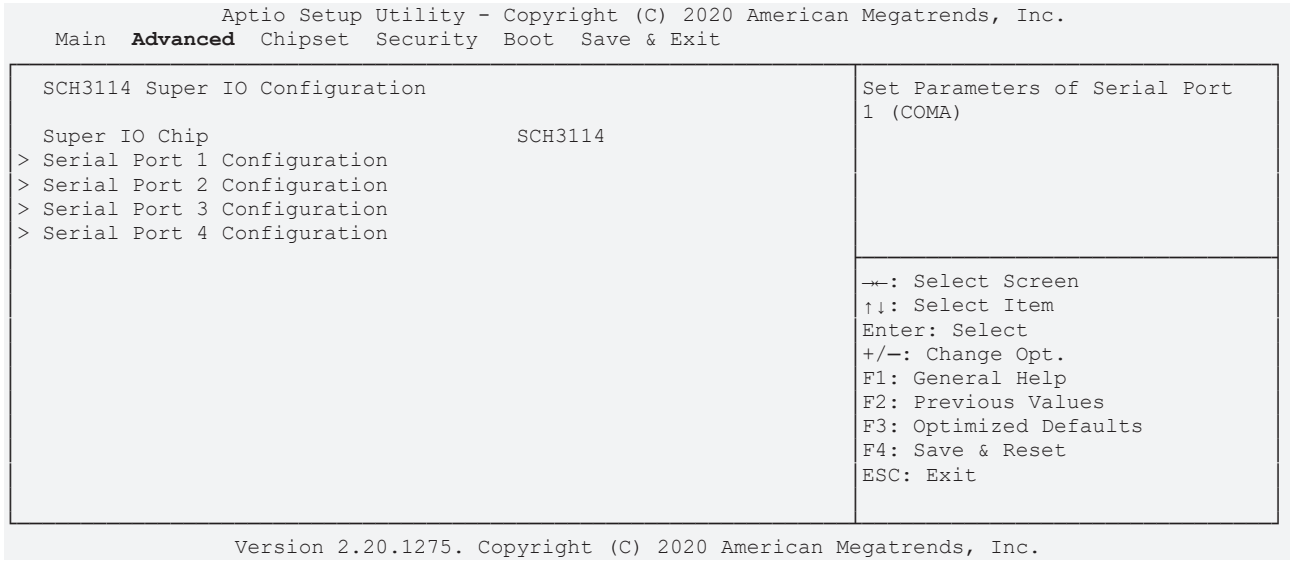


Bios entry	Options
Configuration	
Security Device Support	Enable/Disable
No Security Device Found	None

6.3.4 ACPI Settings Enabled

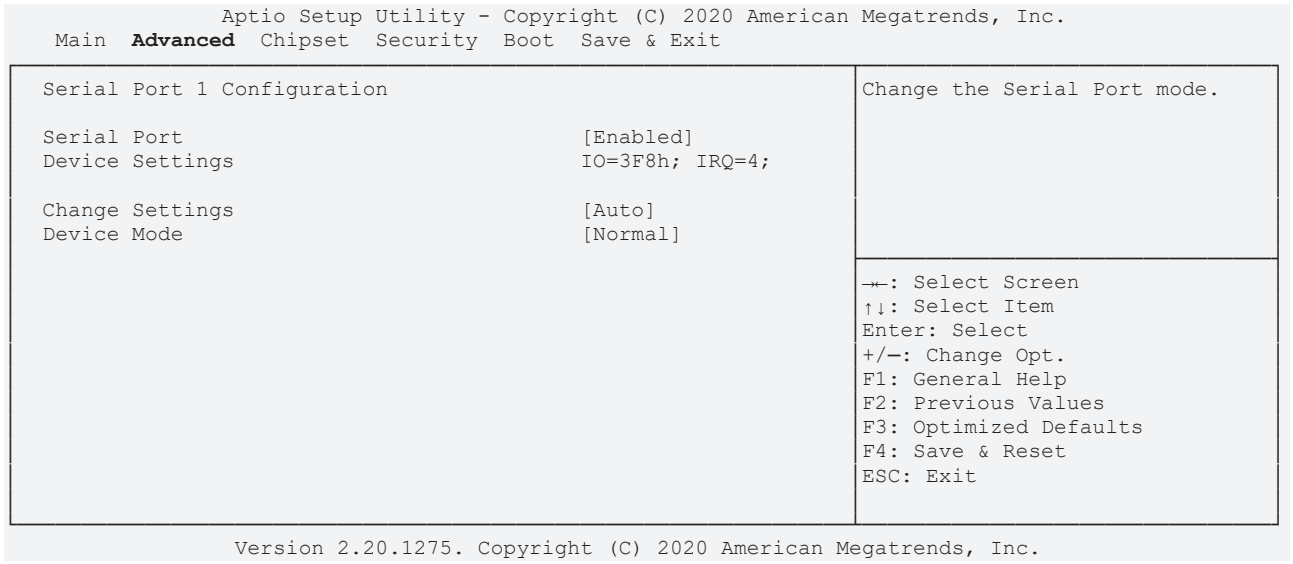
Bios entry	Options
ACPI Settings	
Enable ACPI Auto Configuration	Enabled/Disabled
S3 – Suspend to RAM	None

6.3.5 SCH3114 Super IO Configuration



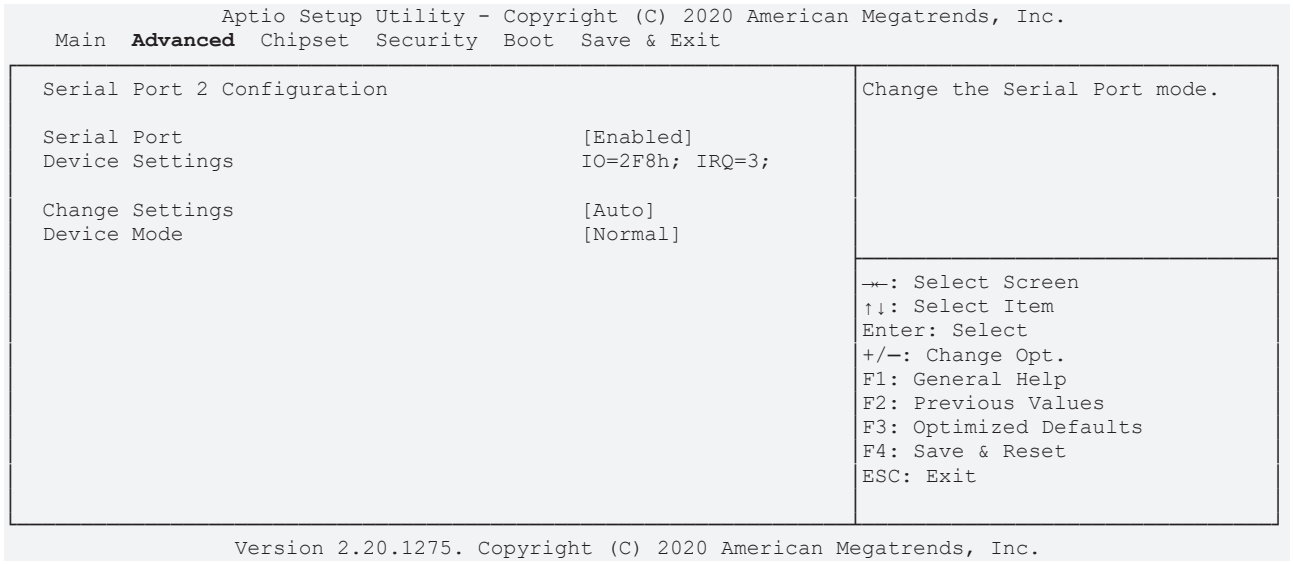
Bios entry	Options
SCH3114 Super IO Configuration	
Super IO Chip	
Serial Port 1 Configuration	Submenu see: Serial Port 1 Configuration [▶ 48]
Serial Port 2 Configuration	Submenu see: Serial Port 2 Configuration [▶ 49]
Serial Port 3 Configuration	Submenu see: Serial Port 3 Configuration [▶ 50]
Serial Port 4 Configuration	Submenu see: Serial Port 4 Configuration [▶ 51]

6.3.5.1 Serial Port 1 Configuration



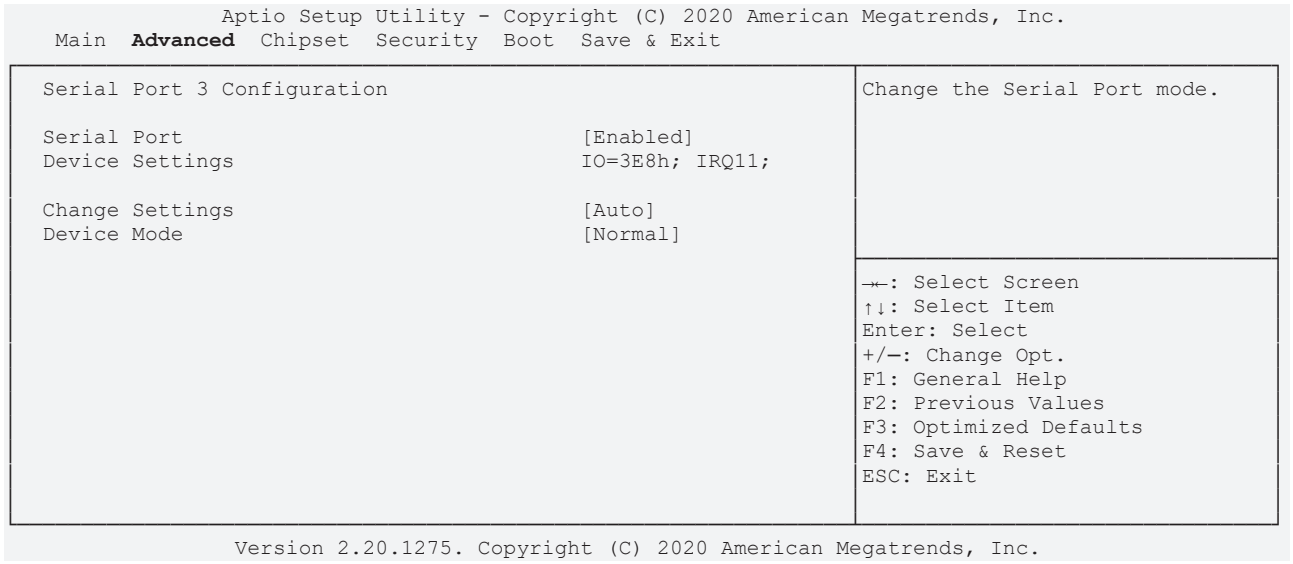
Bios entry	Options
Serial Port 1 Configuration	
Serial Port	Enabled/Disabled
Device Settings	None
Change Settings	Auto/IO=3F8h; IRQ=4;…IO=3F8h; IRQ=3,4,5,6,7,9,10,11,12; and further
Device Mode	Normal/High Speed

6.3.5.2 Serial Port 2 Configuration



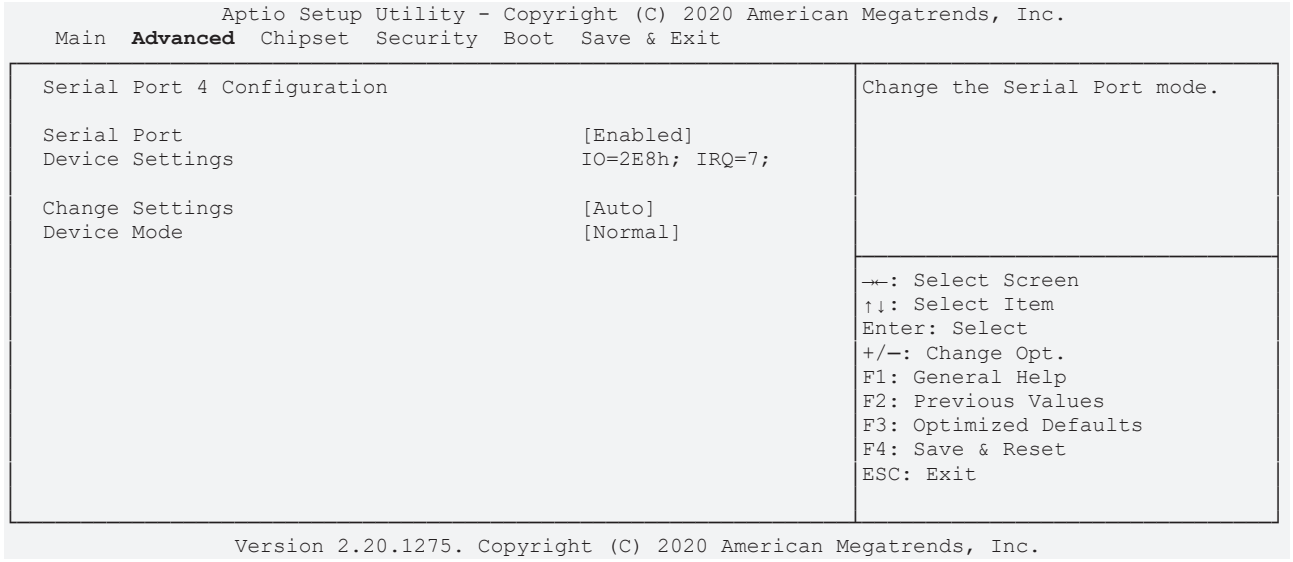
Bios entry	Options
Serial Port 2 Configuration	
Serial Port	Enabled/Disabled
Device Settings	None
Change Settings	Auto/IO=2F8h; IRQ=3;…IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12; and further
Device Mode	Normal/High Speed

6.3.5.3 Serial Port 3 Configuration



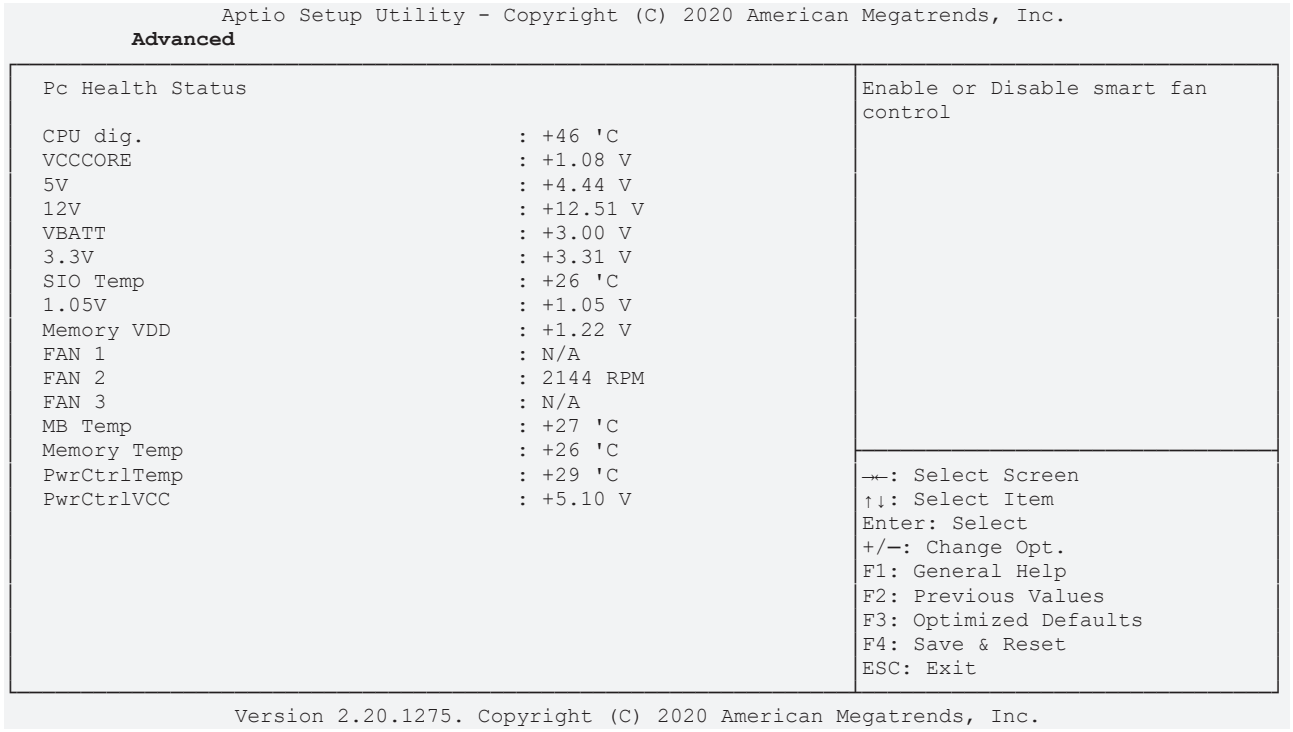
Bios entry	Options
Serial Port 3 Configuration	
Serial Port	Enabled/Disabled
Device Settings	None
Change Settings	Auto/IO=3E8h; IRQ=11;…IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12; and further
Device Mode	Normal/High Speed

6.3.5.4 Serial Port 4 Configuration



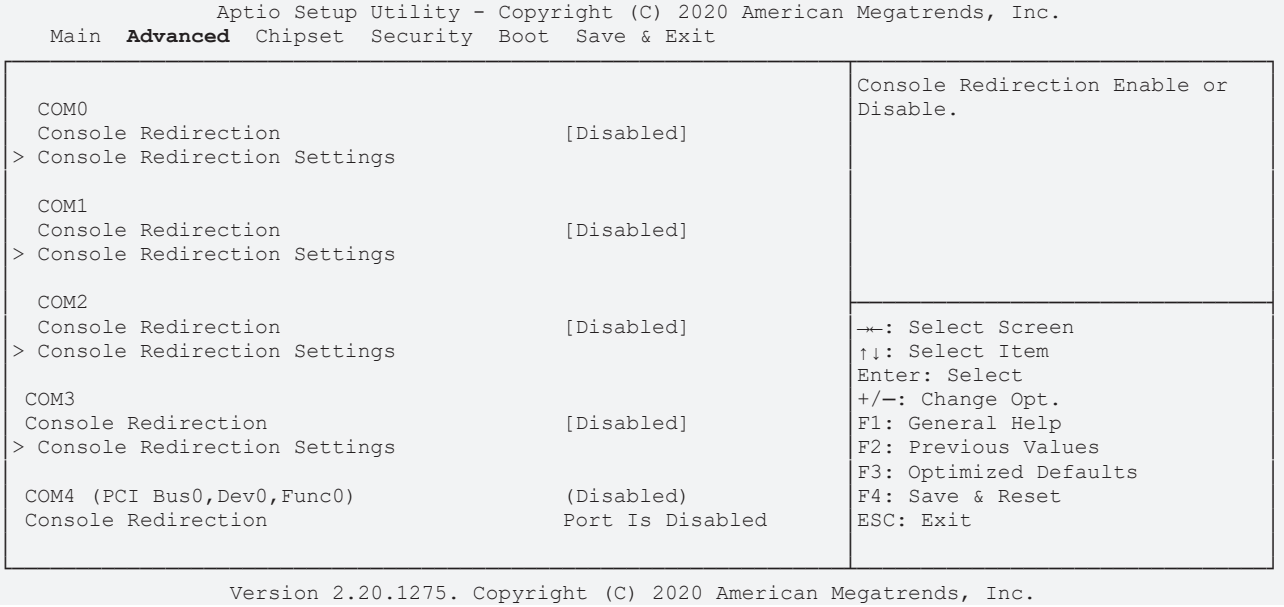
Bios entry	Options
Serial Port 4 Configuration	
Serial Port	Enabled/Disabled
Device Settings	None
Change Settings	Auto/IO=2E8h; IRQ=10;…IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12; and further
Device Mode	Normal/High Speed

6.3.6 Hardware Monitor



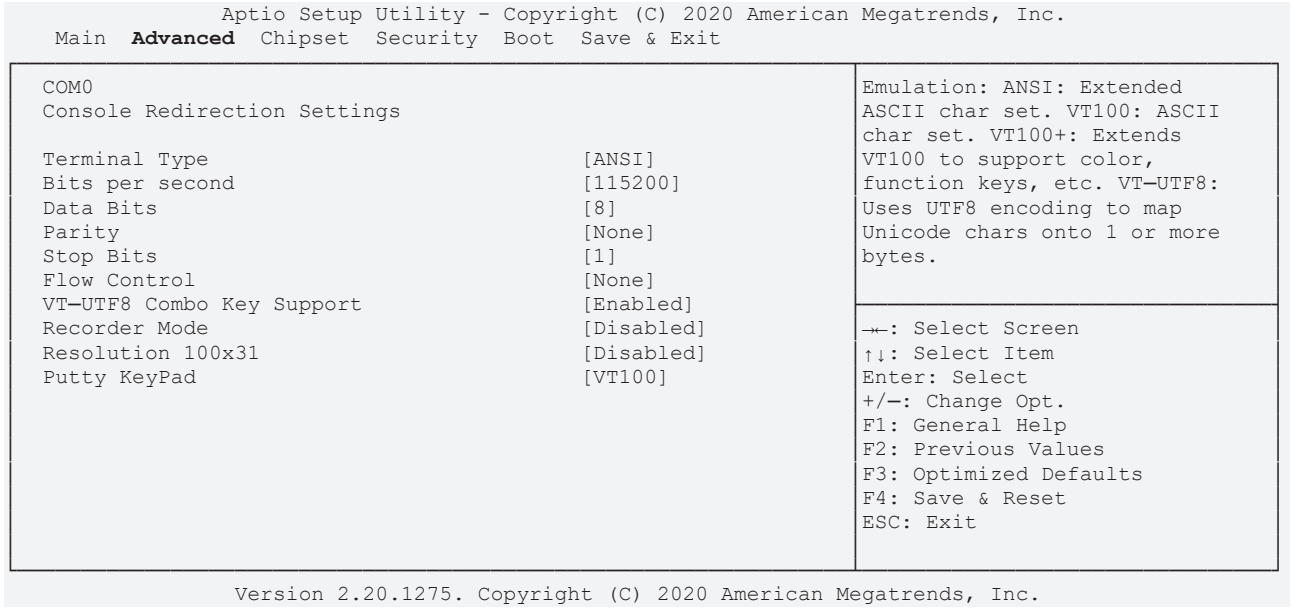
Bios entry	Options
PC Health Status	None

6.3.7 Serial Port Console Redirection



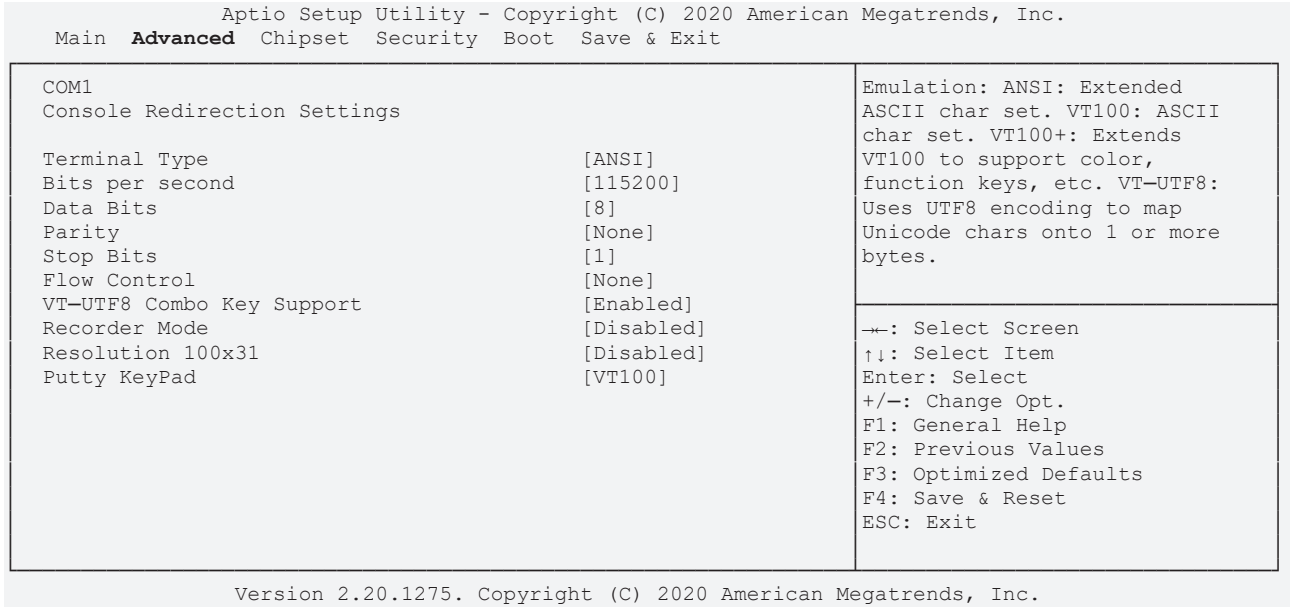
Bios entry	Options
COM0	
Console Redirection	Disabled/Enabled
Console Redirection Settings	Submenu see: COM0 Console Redirection Settings [▶ 54]
COM1	
Console Redirection	Disabled/Enabled
Console Redirection Settings	Submenu see: COM1 Console Redirection Settings [▶ 55]
COM2	
Console Redirection	Disabled/Enabled
Console Redirection Settings	Submenu see: COM2 Console Redirection Settings [▶ 56]
COM3	
Console Redirection	Disabled/Enabled
Console Redirection Settings	Submenu see: COM3 Console Redirection Settings [▶ 57]
COM4 (Pci Bus0, Dev0, Func0) (Disabled)	
Console Redirection	Port Is Disabled

6.3.7.1 COM0 Console Redirection Settings



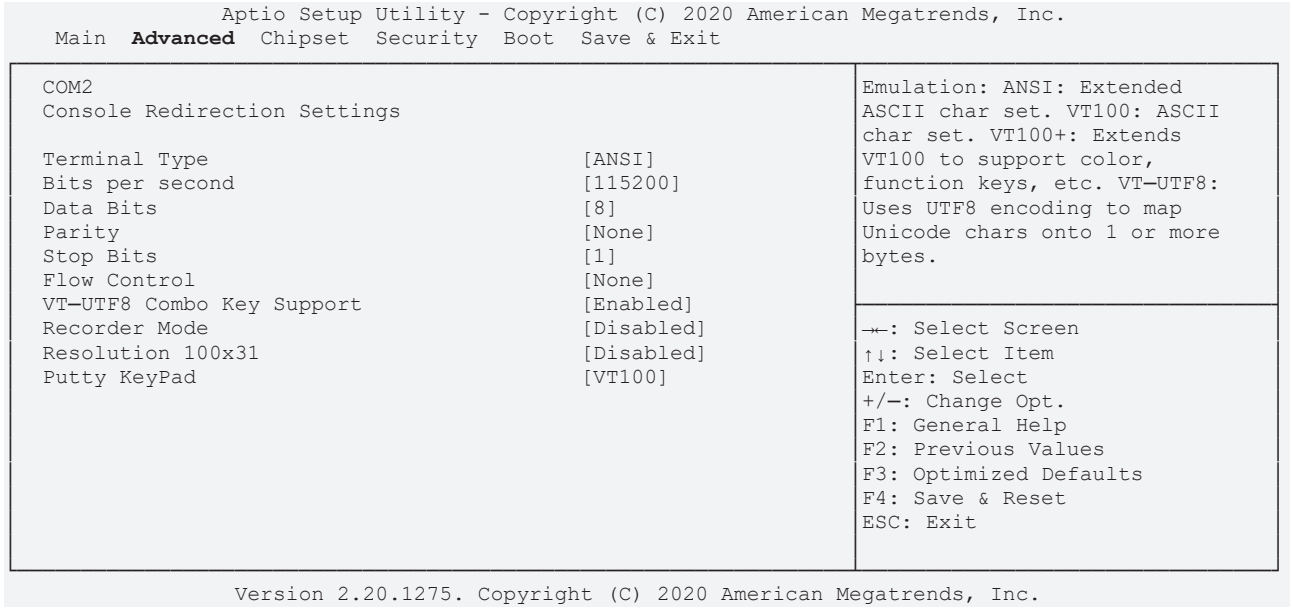
Bios entry	Options
COM0	
Console Redirection Settings	
Serial Port Terminal Type	VT100/VT100+/VT-UTF8/ANSI
Bits per second	9600/19200/38400/57600/115200
Data Bits	7/8
Parity	None/Even/Odd/Mark/Space
Stop Bits	1/2
Flow Control	None/Hardware RTS/CTS
VT-UTF8 Combo Key Support	Enabled/Disabled
Recorder Mode	Disabled/Enabled
Resolution 100x31	Disabled/Enabled
Putty KeyPad	VT100/LINUX/XTERMR6/SCO/ESCN/VT400

6.3.7.2 COM1 Console Redirection Settings



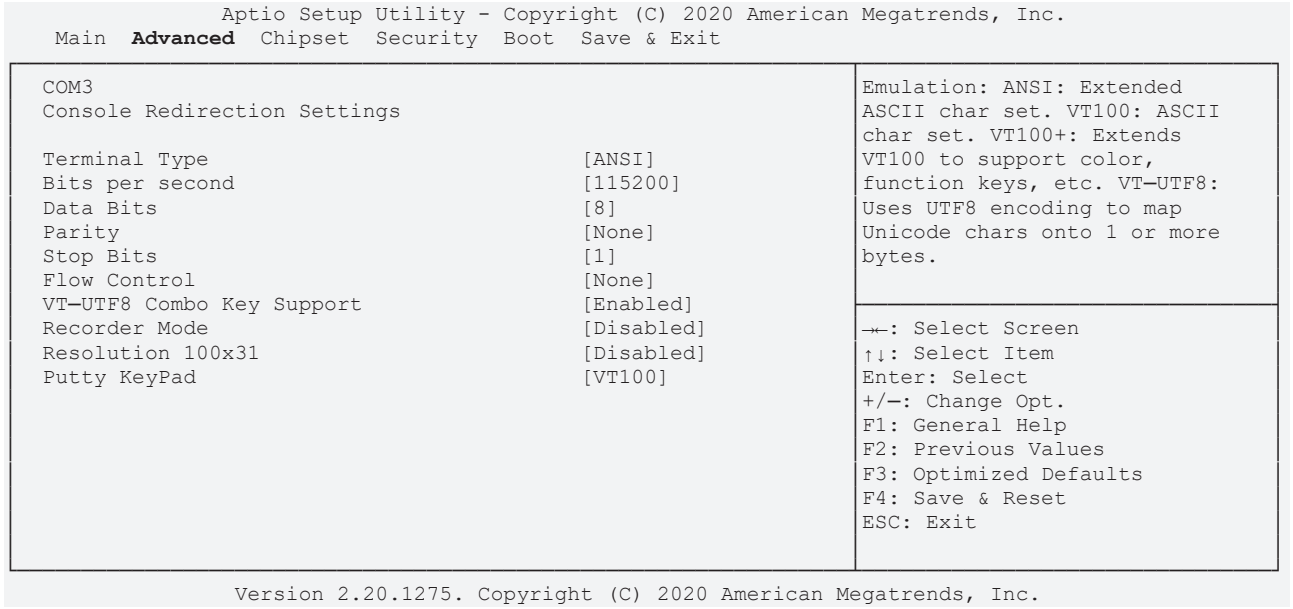
Bios entry	Options
COM1	
Console Redirection Settings	
Serial Port Terminal Type	VT100/VT100+/VT-UTF8/ANSI
Bits per second	9600/19200/38400/57600/115200
Data Bits	7/8
Parity	None/Even/Odd/Mark/Space
Stop Bits	1/2
Flow Control	None/Hardware RTS/CTS
VT-UTF8 Combo Key Support	Enabled/Disabled
Recorder Mode	Disabled/Enabled
Resolution 100x31	Disabled/Enabled
Putty KeyPad	VT100/LINUX/XTERMR6/SCO/ESCN/VT400

6.3.7.3 COM2 Console Redirection Settings



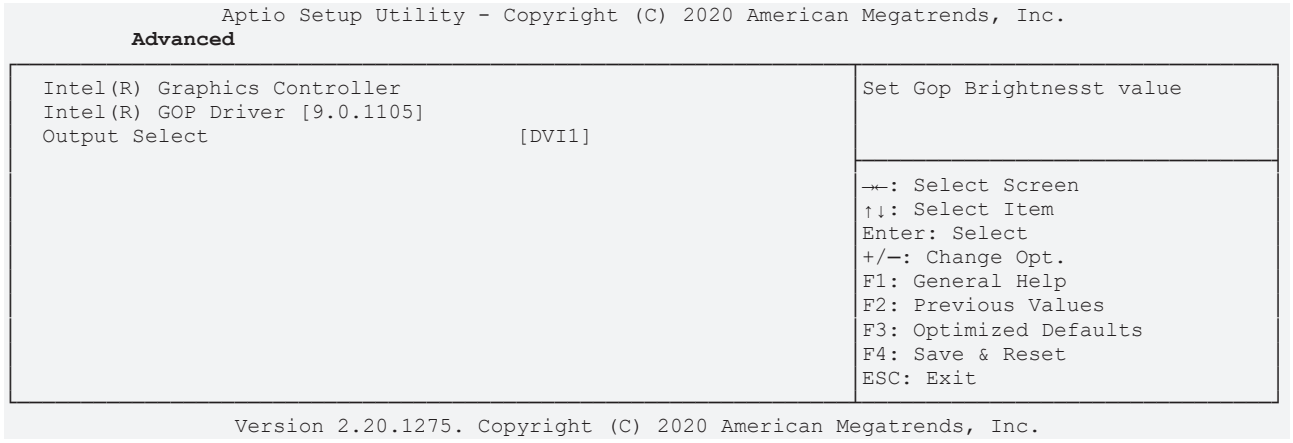
Bios entry	Options
COM2	
Console Redirection Settings	
Serial Port Terminal Type	VT100/VT100+/VT-UTF8/ANSI
Bits per second	9600/19200/38400/57600/115200
Data Bits	7/8
Parity	None/Even/Odd/Mark/Space
Stop Bits	1/2
Flow Control	None/Hardware RTS/CTS
VT-UTF8 Combo Key Support	Enabled/Disabled
Recorder Mode	Disabled/Enabled
Resolution 100x31	Disabled/Enabled
Putty KeyPad	VT100/LINUX/XTERMR6/SCO/ESCN/VT400

6.3.7.4 COM3 Console Redirection Settings



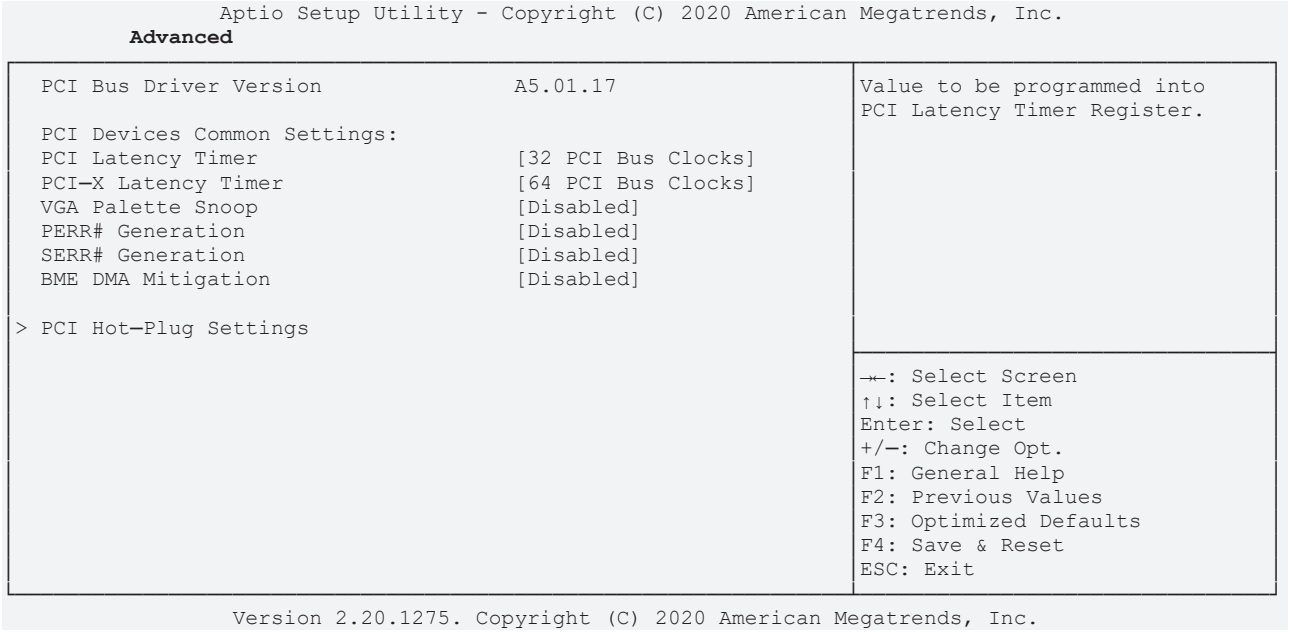
Bios entry	Options
COM3	
Console Redirection Settings	
Serial Port Terminal Type	VT100/VT100+/VT-UTF8/ANSI
Bits per second	9600/19200/38400/57600/115200
Data Bits	7/8
Parity	None/Even/Odd/Mark/Space
Stop Bits	1/2
Flow Control	None/Hardware RTS/CTS
VT-UTF8 Combo Key Support	Enabled/Disabled
Recorder Mode	Disabled/Enabled
Resolution 100x31	Disabled/Enabled
Putty KeyPad	VT100/LINUX/XTERMR6/SCO/ESCN/VT400

6.3.8 AMI Graphic Output Protocol Policy



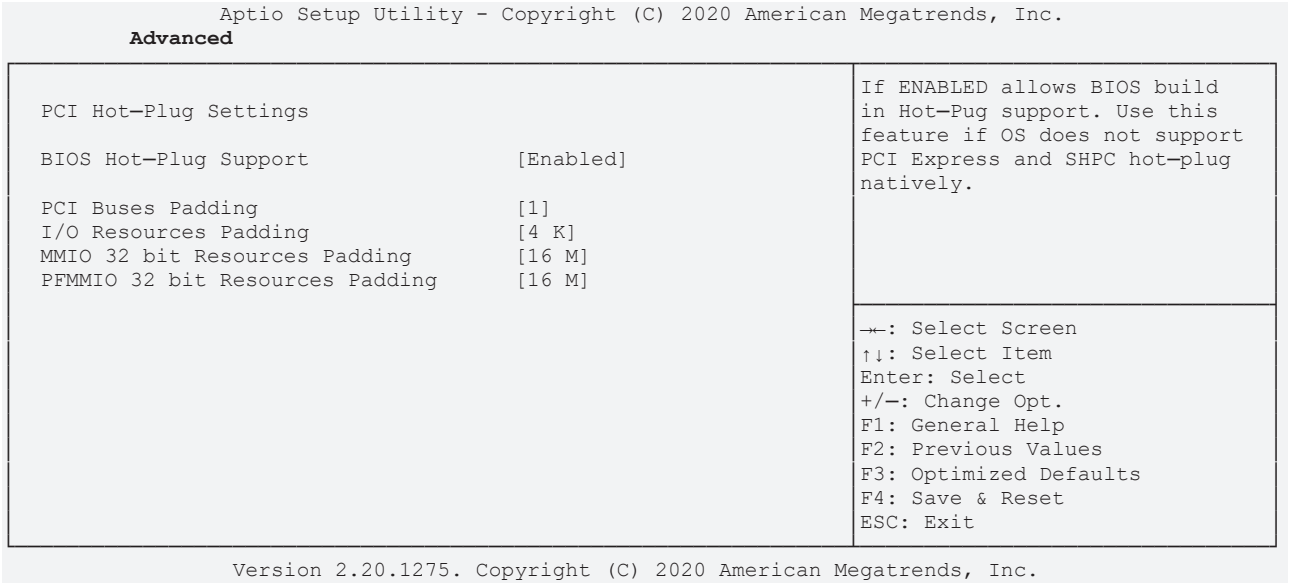
Bios entry	Options
Intel® Graphics Controller Intel® GOP Driver [9.0.1105]	
Output Select	None

6.3.9 PCI Subsystem Settings



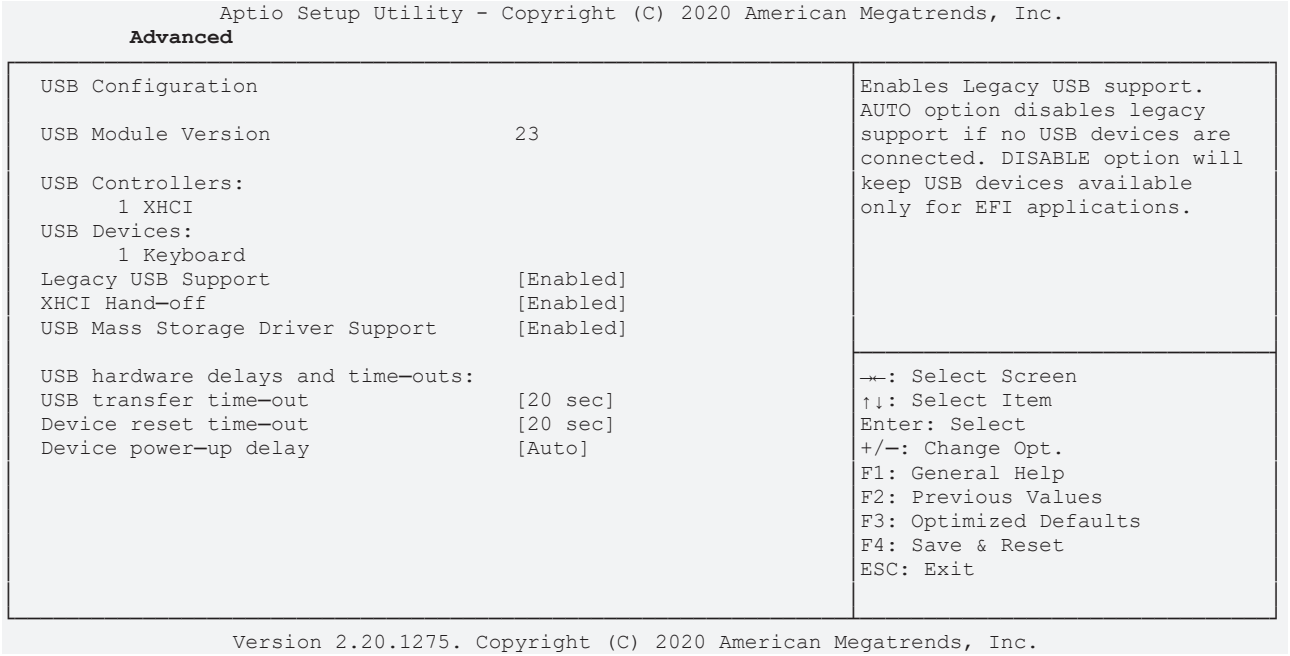
Bios entry	Options
PCI Bus Driver Version	None
PCI Device Common Settings:	
PCI Latency Timer	32/64/96/128/160/192/224/248/PCI Bus Clocks
PCI-X Latency Timer	32/64/96/128/160/192/224/248/PCI Bus Clocks
VGA Palette Snoop	Disabled/Enabled
PERR# Generation	Disabled/Enabled
SERR# Generation	Disabled/Enabled
BME DMA Mitigation	Disabled/Enabled
PCI Hot-Plug Settings	Submenu see: PCI Hot-Plug Settings [▶ 60]

6.3.9.1 PCI Hot-Plug Settings



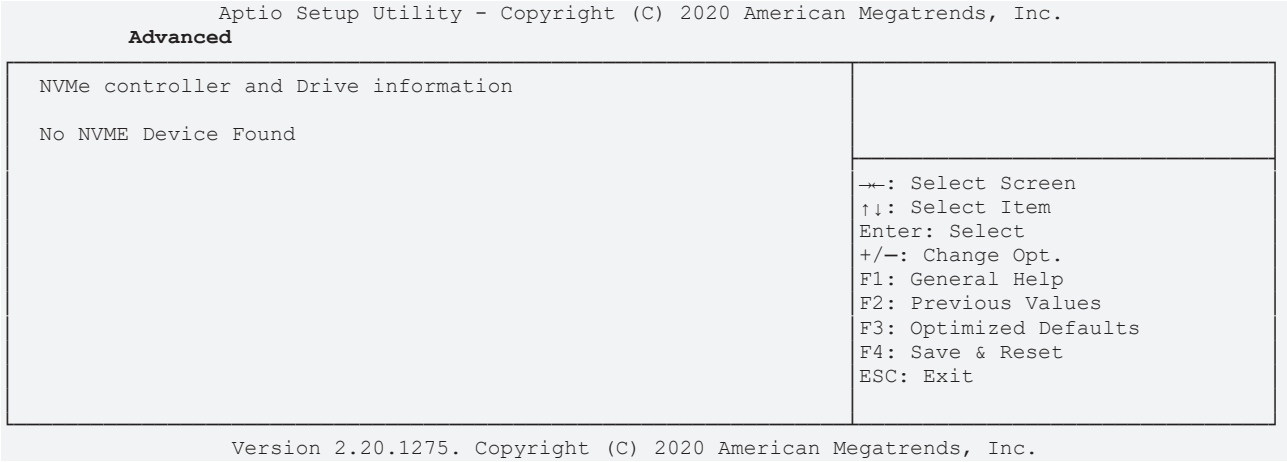
Bios entry	Options
PCI Hot-Plug Settings	
BIOS Hot-Slug support	Enabled/Disabled
PCI Buses Padding	Disabled/1/2/3/4/5
I/O Resources Padding	Disabled/4 K/8 K/16 K/32 K
MMIO 32 bit Resources Padding	Disabled/1 M/2 M/4 M/ 8 M/16 M/32 M/64 M/128 M
PFMMIO 32 bit Resources Padding	Disabled/1 M/2 M/4 M/8 M/16 M/32 M/64 M/128 M

6.3.10 USB Configuration



Bios entry	Options
USB Configuration	
USB Module Version	None
USB Controllers: 1XHCI	None
USB Devices: 1 Keyboard	None
Legacy USB Support	Enabled/Disabled/Auto
XHCI Hand-off	Enabled/Disabled
USB Mass Storage Driver Support	Enabled/Disabled
USB hardware delays and time-outs:	
USB transfer time-out	1/5/10/20 sec
Device reset time-out	10/20/30/40 sec
Device power-up delay	Auto/Manual

6.3.11 NVMe Configuration

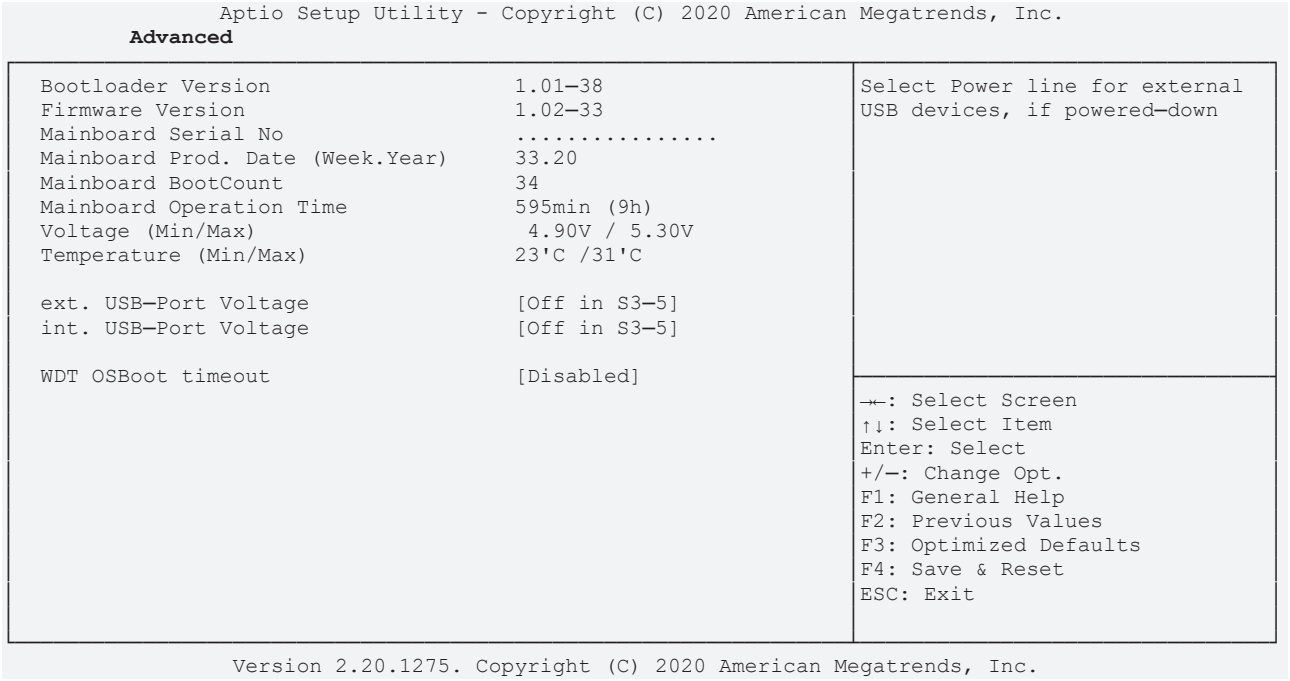


Bios entry	Options
NVMe controller and Drive information	
No NVME Device Found	None

NOTE

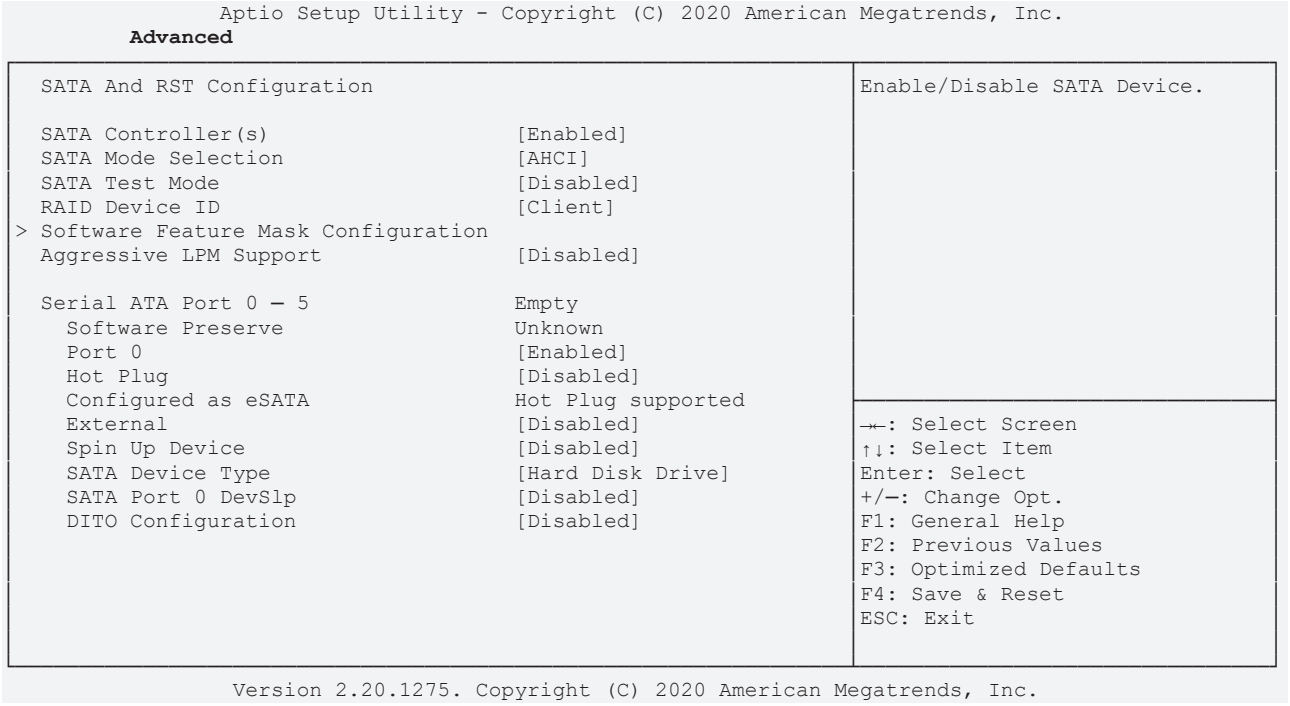
NVMe Raid 0/1 is not supported.

6.3.12 Power Controller Options



Bios entry	Options
Bootloader Version	None
Firmware Version	None
Mainboard Serial No	None
Mainboard Prod. Date (Week.Year)	None
Mainboard BootCount	None
Mainboard Operation Time	None
Voltage /Min/Max)	None
Temperature (Min/Max)	None
ext. USB port Voltage	Off in S3-5/by SCVV
int. USB port Voltage	Off in S3-5/by SCVV
WDT OSBoot Timeout	Disabled/45/60/.../255 Seconds

6.3.13 SATA And RST Configuration



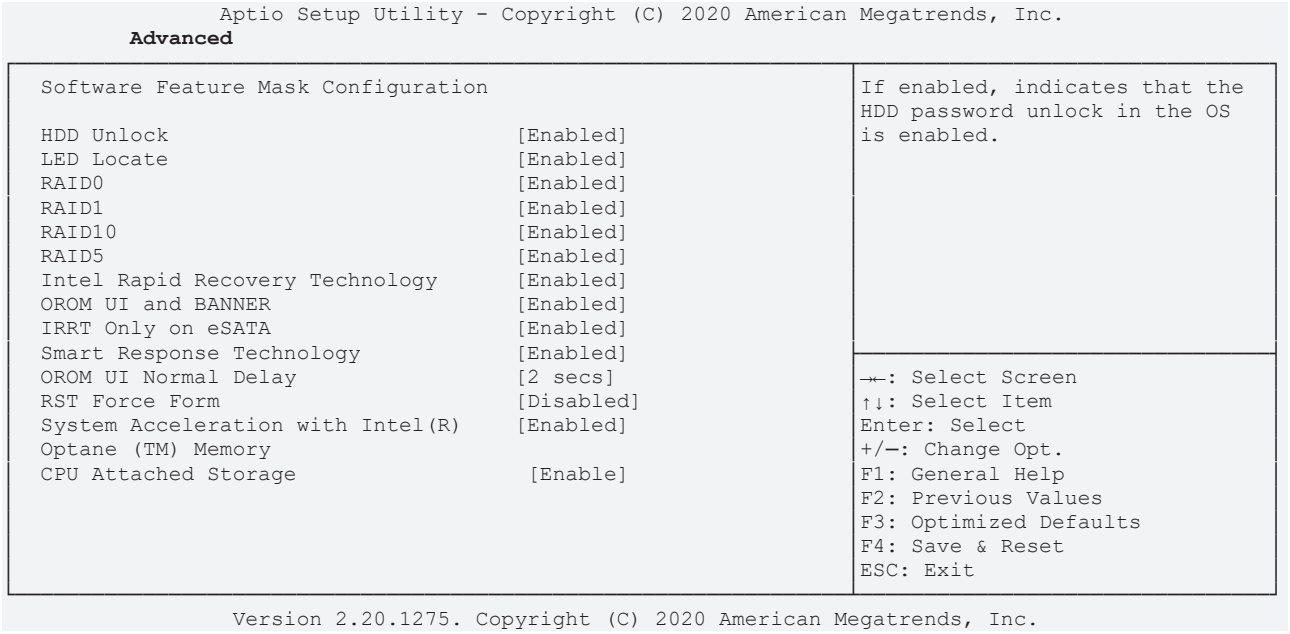
Bios entry	Options
SATA And RST Configuration	
SATA controller(s)	Enabled/Disabled
SATA Mode Selection	AHCI/Intel RST Premium With Intel Optane System acceleration
SATA Test Mode	Disabled/Enabled
Software Feature Mask Configuration	Submenu see: Software Feature Mask Configuration [▶ 65]
Aggressive LPM support	Disabled/Enabled
Serial ATA port 0 - 5	None
Software Preserve	None
Port 0	Disabled/Enabled
Hot Plug	Disabled/Enabled
Configured as eSATA	None
External	Disabled/Enabled
Spin Up Device	Disabled/Enabled
SATA Device Type	HDD/SSD
SATA Port 0 DevSlp	Disabled/Enabled
DITO Configuration	Disabled/Enabled

NOTE

Settings on SATA ports 0 - 5

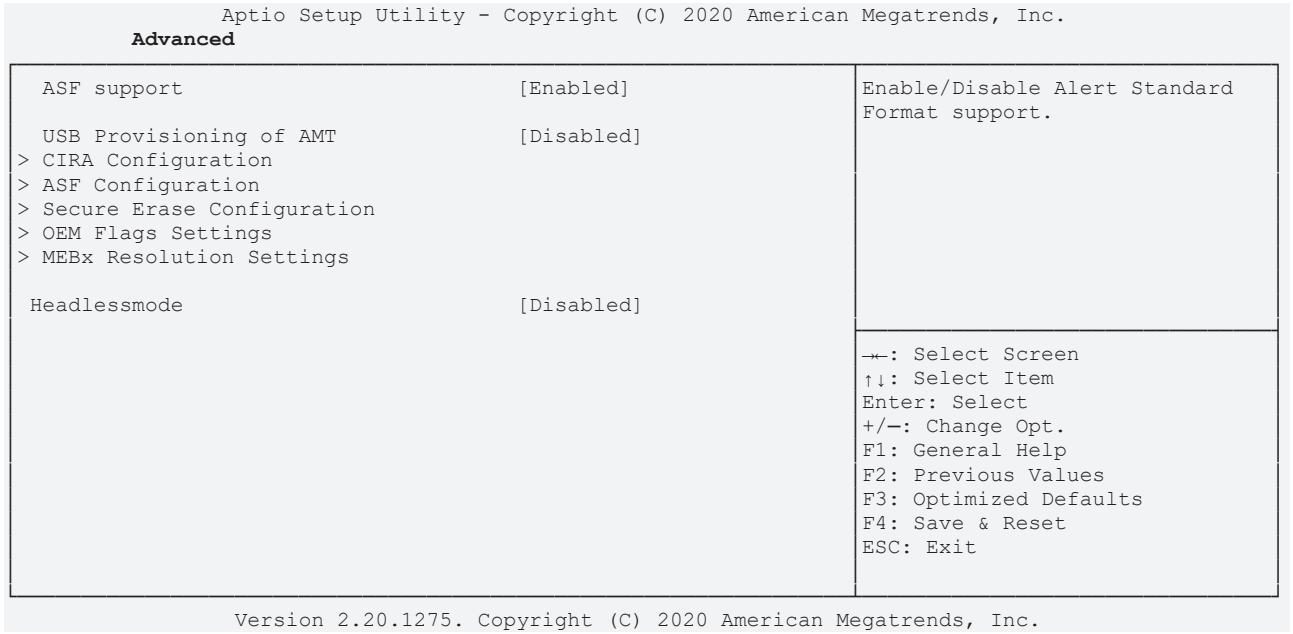
The possible settings on SATA ports 0-5 are identical. Therefore, these are summarized in the illustration.

6.3.13.1 Software Feature Mask Configuration



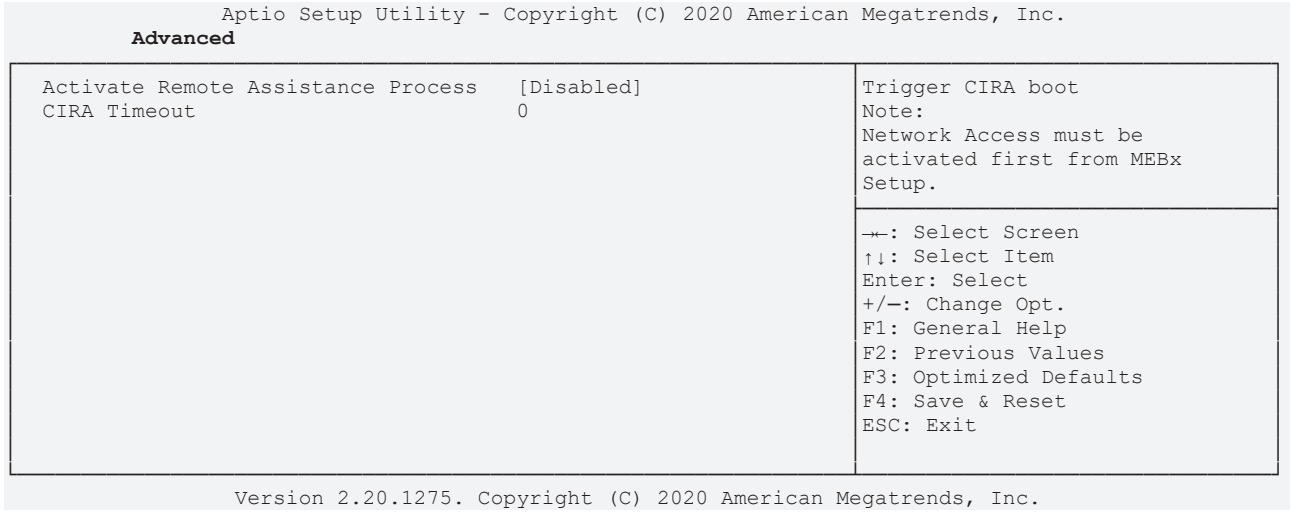
Bios entry	Options
Software Feature Mask Configuration	
HDD Unlock	Enabled/Disabled
LED Locate	Enabled/Disabled
RAID0	Enabled/Disabled
RAID1	Enabled/Disabled
RAID10	Enabled/Disabled
RAID5	Enabled/Disabled
Intel Rapid Recovery Technology	Enabled/Disabled
OROM UI and BANNER	Enabled/Disabled
IRRT Only on eSATA	Enabled/Disabled
Smart Response Technology	Enabled/Disabled
OROM UI Normal Delay	2/4/6/8 secs
RST Force Norm	Disabled/Enabled
System Acceleration with Intel(R) Optane(TM) Memory	Enabled/Disabled
CPU Attached Store	Enabled/Disabled

6.3.14 AMT Configuration



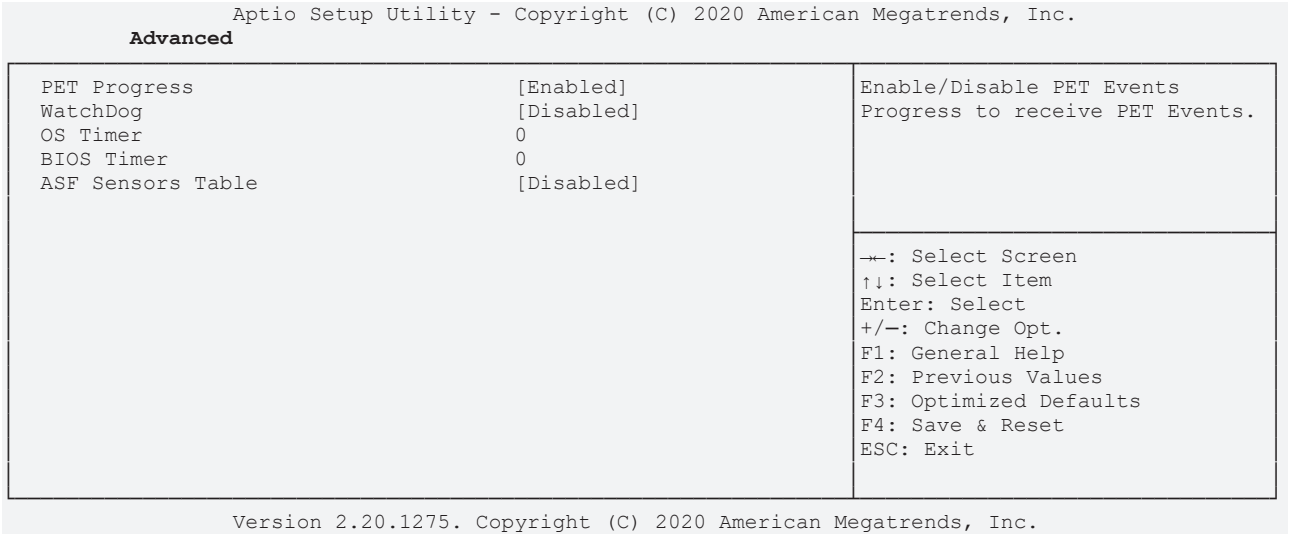
Bios entry	Options
ASF Support	Disabled/Enabled
USB Provisioning of AMT	Disabled/Enabled
CIRA Configuration	Submenu see: CIRA Configuration [▶ 67]
ASF Configuration	Submenu see: ASF Configuration [▶ 68]
Secure Erase Configuration	Submenu see: Secure Erase Configuration [▶ 68]
OEM Flags Settings	Submenu see: OEM Flags Settings [▶ 69]
MEBx Resolution Settings	Submenu see: MEBx Resolution Settings [▶ 70]
Headless mode	Disabled/Enabled

6.3.14.1 CIRA Configuration



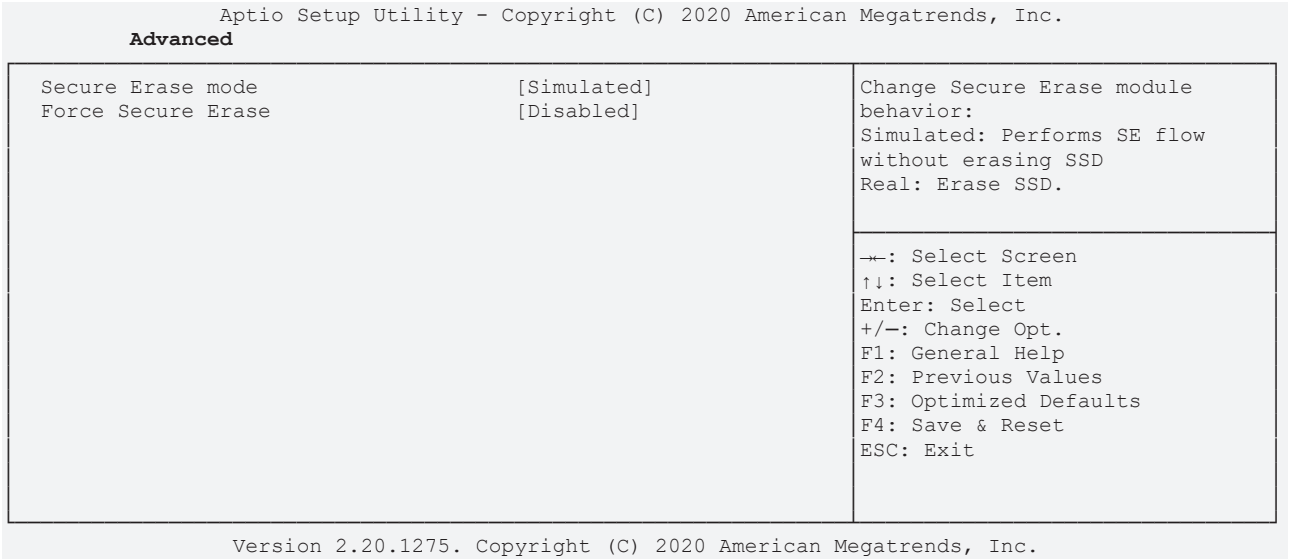
Bios entry	Options
Activate Remote Assistance Process	Disabled/Enabled
CIRA Timeout	None

6.3.14.2 ASF Configuration



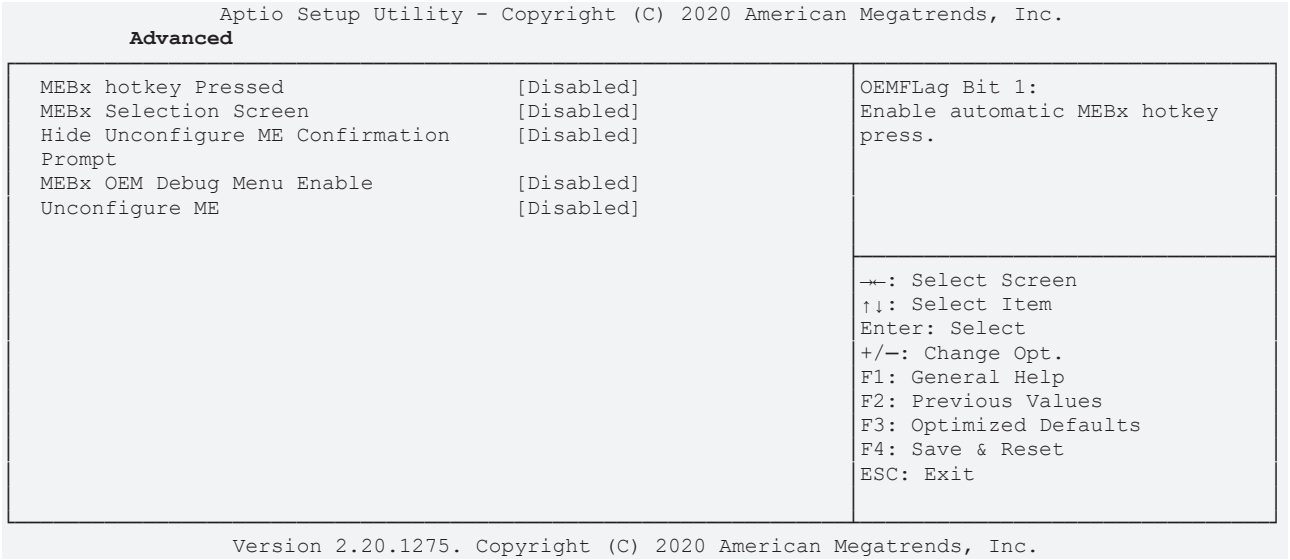
Bios entry	Options
PET Progress	Disabled/Enabled
WatchDog	Disabled/Enabled
OS Timer	None
BIOS Timer	None
ASF Sensors Table	Disabled/Enabled

6.3.14.3 Secure Erase Configuration



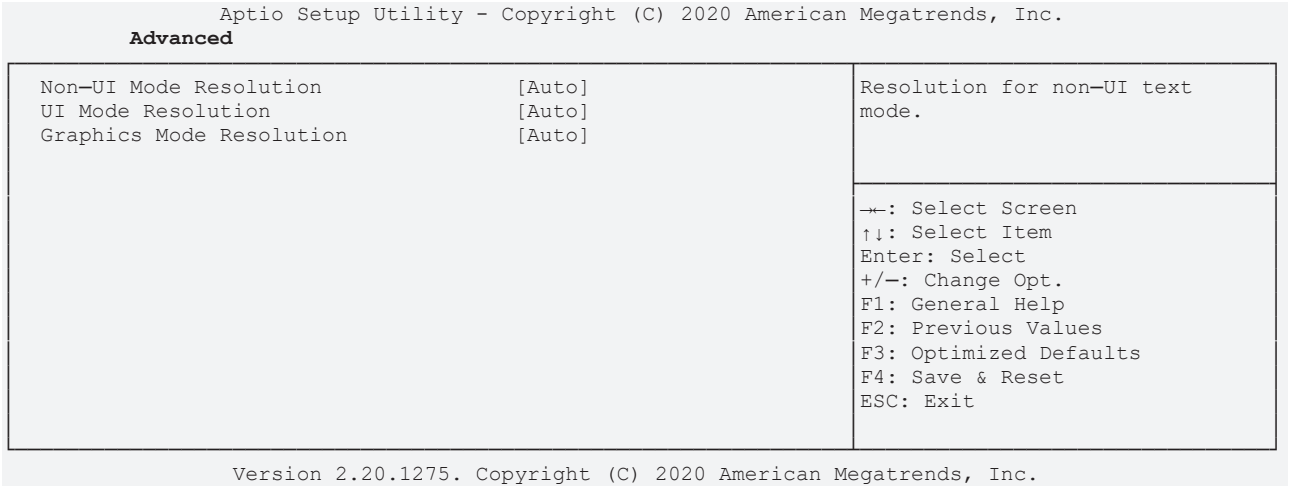
Bios entry	Options
Secure Erase Mode	Simulated/Real
Force Secure Erase	Disabled/Enabled

6.3.14.4 OEM Flags Settings



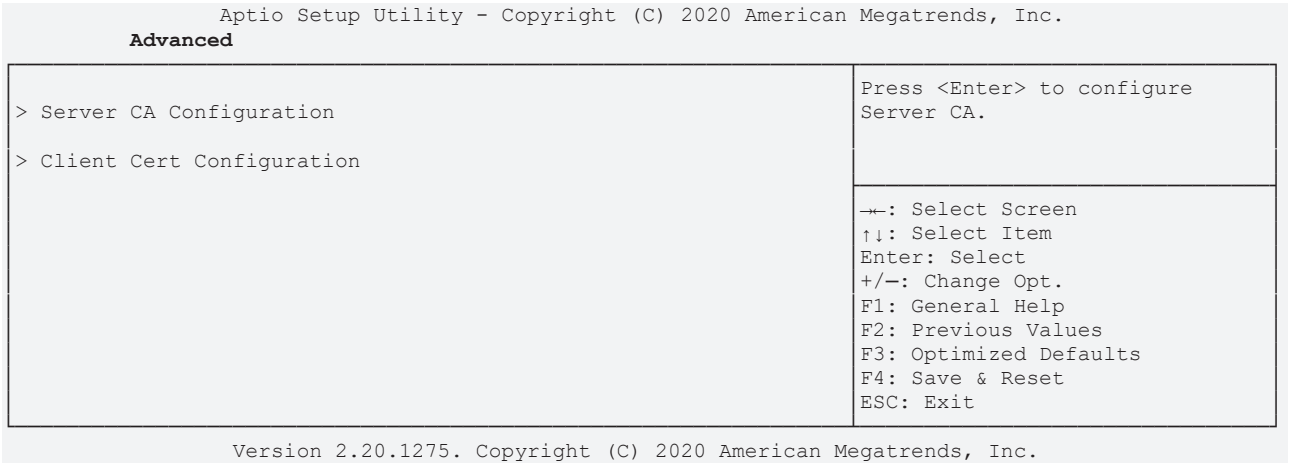
Bios entry	Options
MBEx hotkey Pressed	Disabled/Enabled
MBEx Selection Screen	Disabled/Enabled
Hide Unconfigure ME Confirmation Prompt	Disabled/Enabled
MBEx OEM Debug Menu Enable	Disabled/Enabled
Unconfigure ME	Disabled/Enabled

6.3.14.5 MEBx Resolution Settings



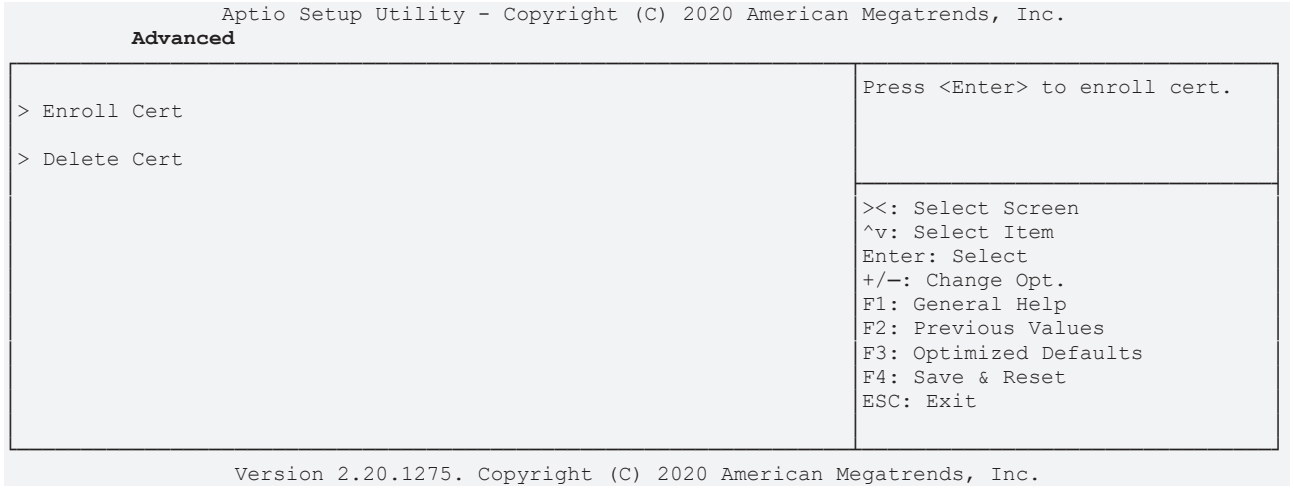
Bios entry	Options
Non-UI Resolution	Auto/80x25/100x31
UI Mode Resolution	Auto/80x25/100x31
Graphics Mode Resolution	Auto/640x480/800x600/1024x768

6.3.15 TLs Auth Configuration



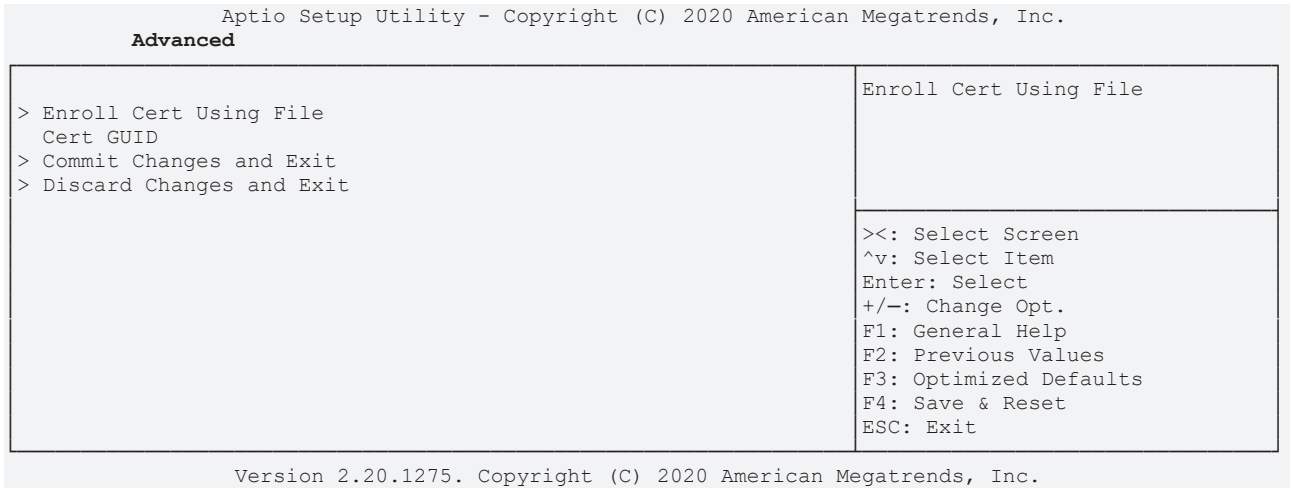
Bios entry	Options
Server CA Configuration	Submenu see: Server CA Configuration [▶ 71]
Client Cert Configuration	None

6.3.15.1 Server CA Configuration



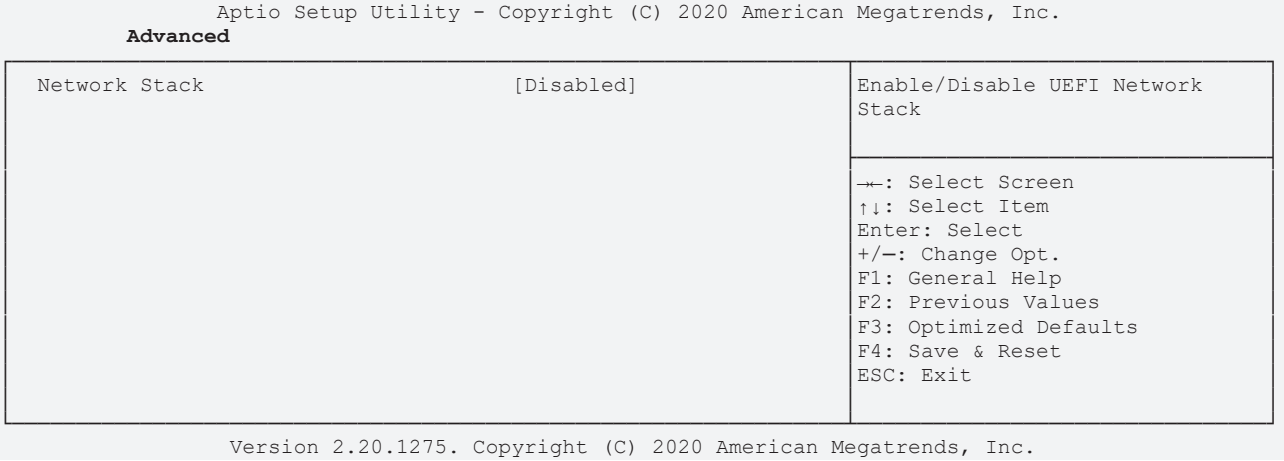
Bios entry	Options
Enroll Cert	Submenu see: Enroll Cert [▶ 71]
Delete Cert	None

6.3.15.1.1 Enroll Cert



Bios entry	Options
Enroll CertEnroll Cert Using File	None
Cert GUID	None
Commit Changes and Exit	None
Discard Changes and Exit	None

6.3.16 Network Stack Configuration



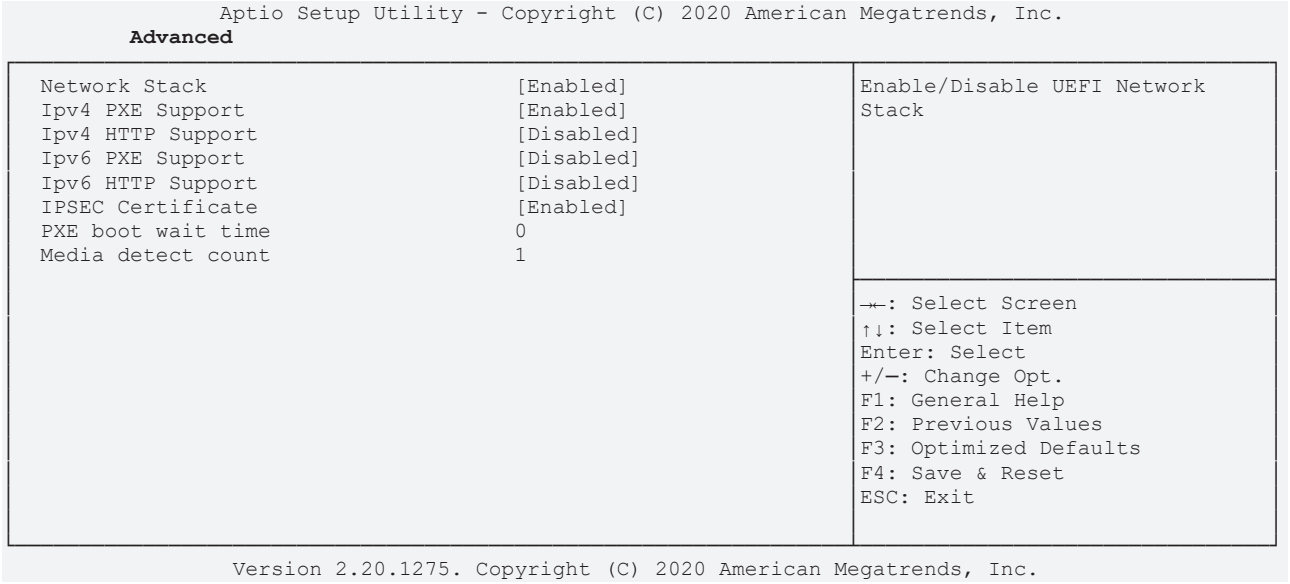
Bios entry	Options
Network Stack	Disabled/Enabled

NOTE

Network Stack Enabled

If Network Stack is enabled, additional menu items for displaying and setting the LAN controllers are shown here. To do this, carry out a reset.

6.3.17 Network Stack Configuration enabled



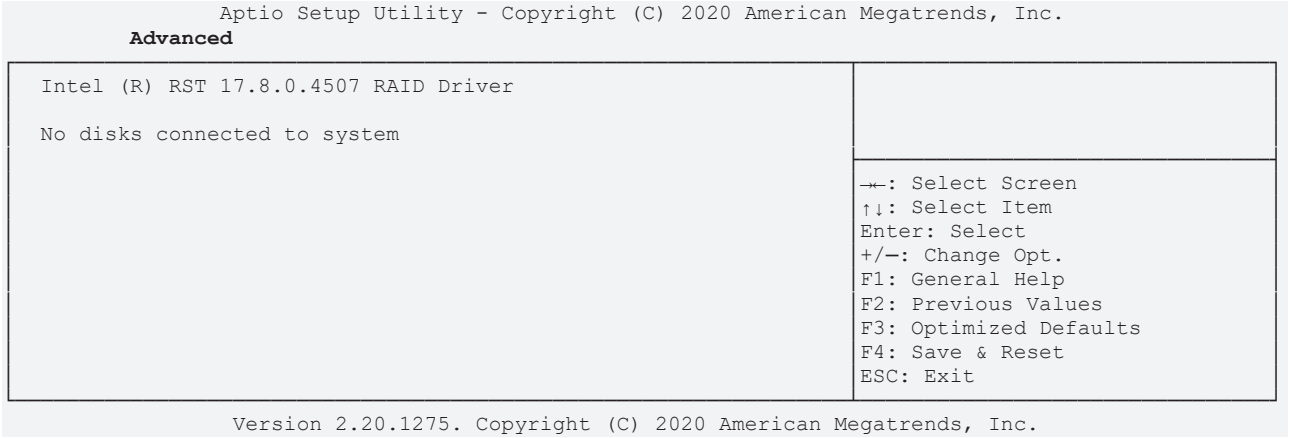
Bios entry	Options
Network Stack	Disabled/Enabled
Ipv4 PXE Support	Disabled/Enabled
Ipv4 HTTP Support	Disabled/Enabled
Ipv6 PXE Support	Disabled/Enabled
Ipv6 HTTP Support	Disabled/Enabled
IPSEC Certificate	Enabled/Disabled
PXE boot wait time	None
Media detect count	None

NOTE

PXE Boot available

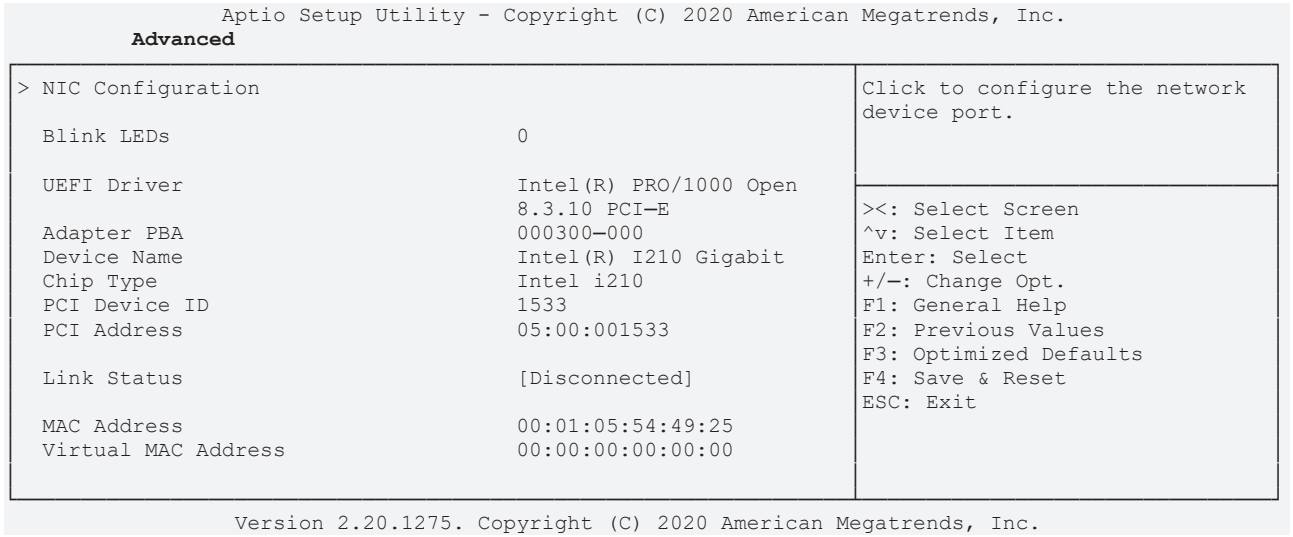
PXE Boot is available if you set Network Stack and Ipv4 PXE support to "Enable".

6.3.18 Intel Rapid Storage Technology



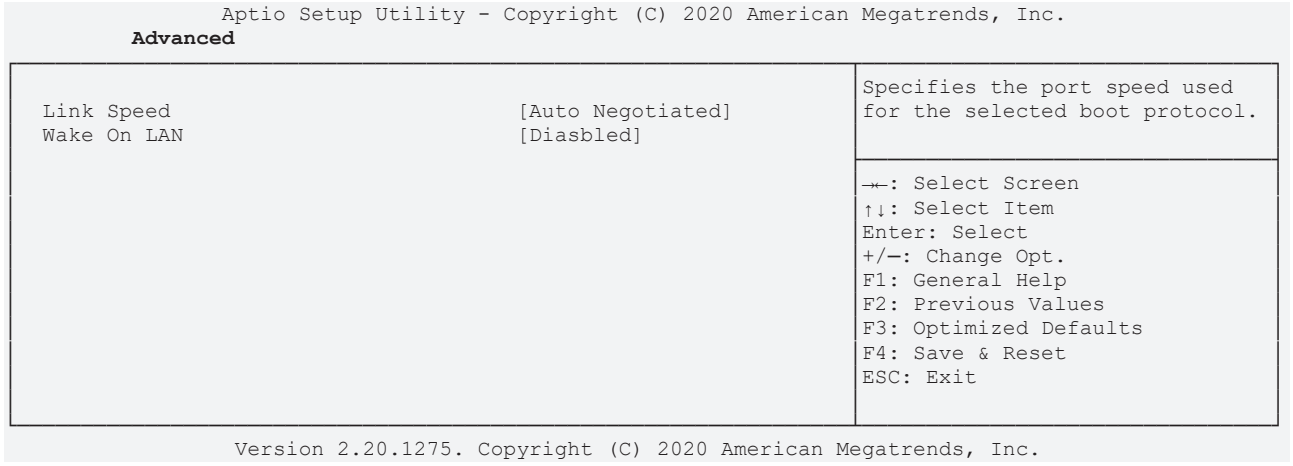
Bios entry	Options
Intel® RST 17.8.0.4507 RAID Driver	
No disks connected to system	None

6.3.19 Intel I210 Gigabit Network Connection



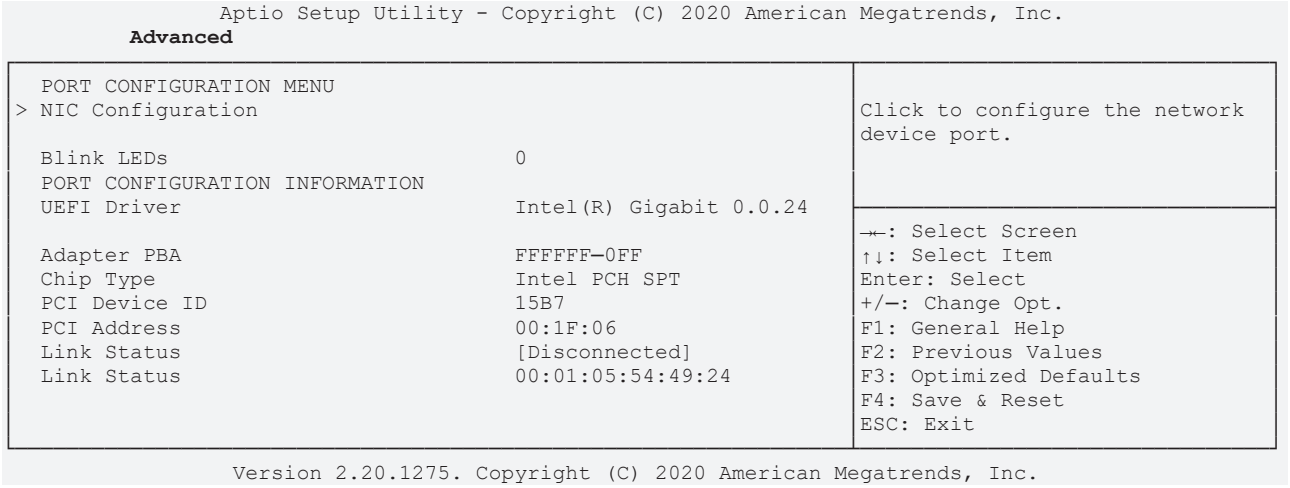
Bios entry	Options
NIC Configuration	Submenu see: NIC Configuration [▶ 75]
Flashing LEDs	None
UEFI driver	None
PBA adapter	None
Device Name	None
Chip type	None
PCI Device ID	None
PCI Address	None
Link status	None
MAC Address	None
Virtual MAC Address	None

6.3.19.1 NIC Configuration



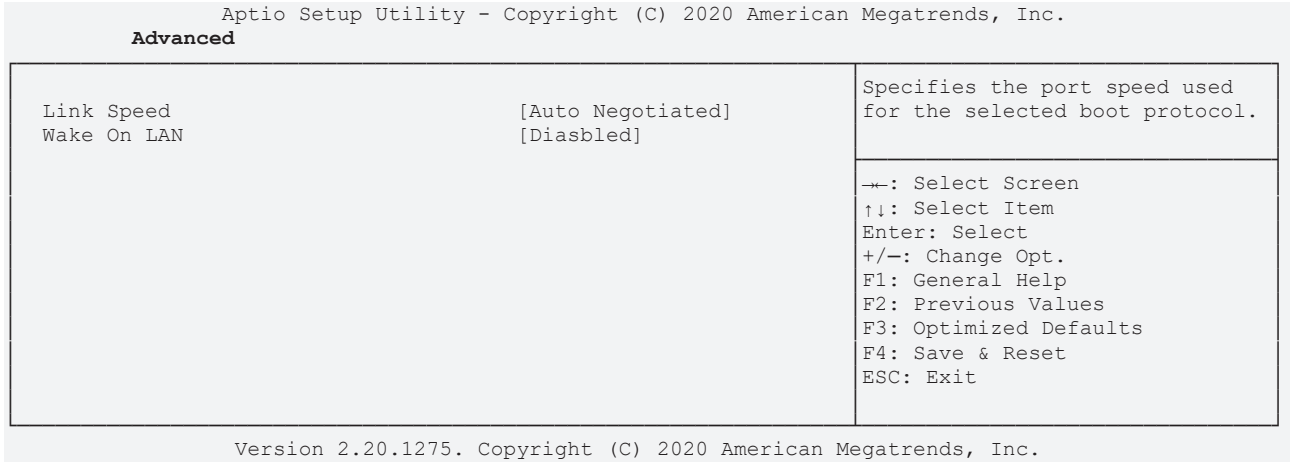
Bios entry	Options
Link Speed	Auto Negotiated/10 Mbps Half/10 Mbps Full/ 100 Mbps Half/100 Mbps Full
Wake On LAN	Disabled/Enabled

6.3.20 Intel Ethernet Connection(2) I219-LM



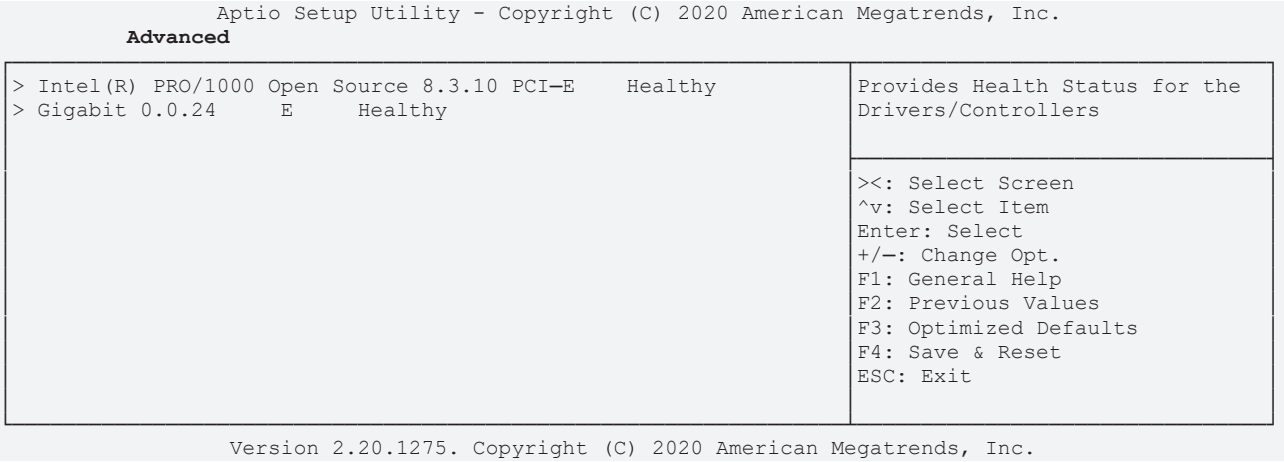
Bios entry	Options
PORT CONFIGURATION MENU	
NIC Configuration	See submenu: NIC Configuration [▶ 77]
Blink LEDs	None
PORT CONFIGURATION INFORMATION	
UEFI Driver	None
Adapter PBA:	None
Chip Type	None
PCI Device ID	None
PCI Address	None
Link Status	None
MAC Address	None

6.3.20.1 NIC Configuration



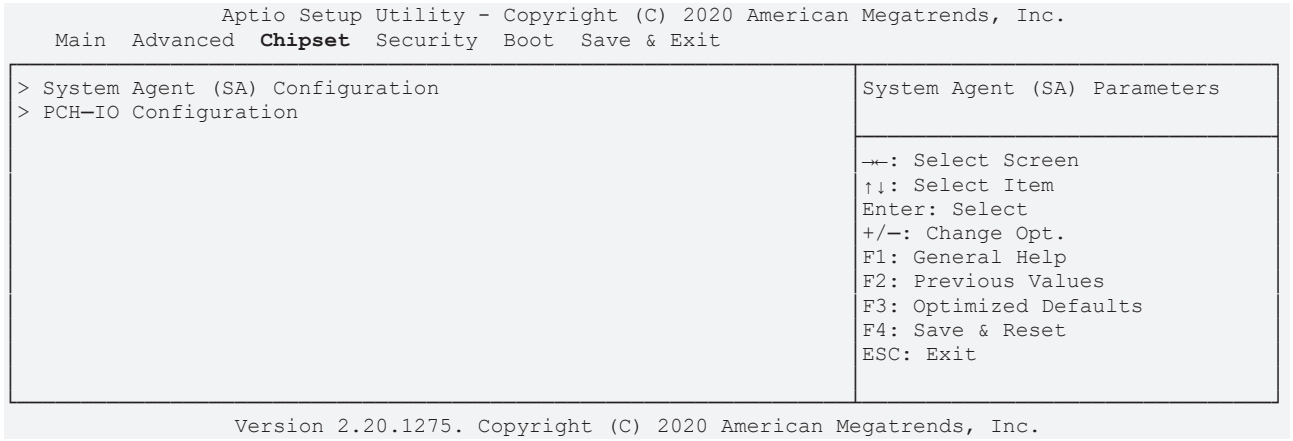
Bios entry	Options
Link Speed	Auto Negotiated/10 Mbps Half/10 Mbps Full/ 100 Mbps Half/100 Mbps Full
Wake On LAN	Disabled/Enabled

6.3.21 Driver Health



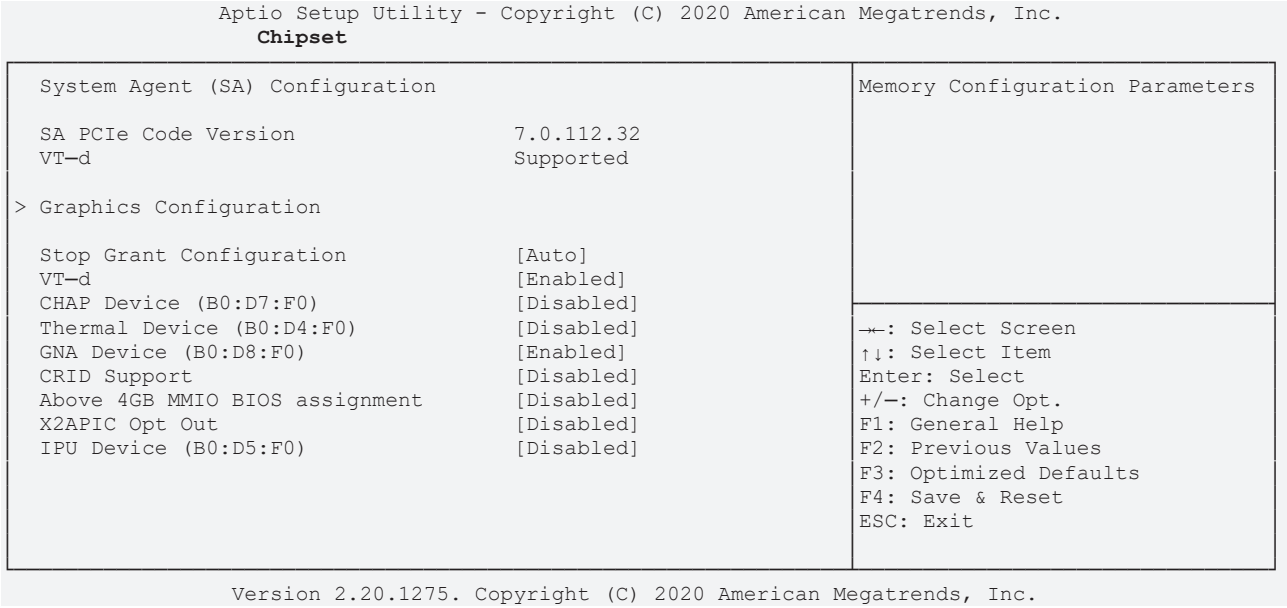
Bios entry	Options
Intel(R) PRO/1000 Open Source 8.3.10 PCI-E Healthy	None
Intel(R) Gigabit 0.0.24 Healthy	None

6.4 Chipset



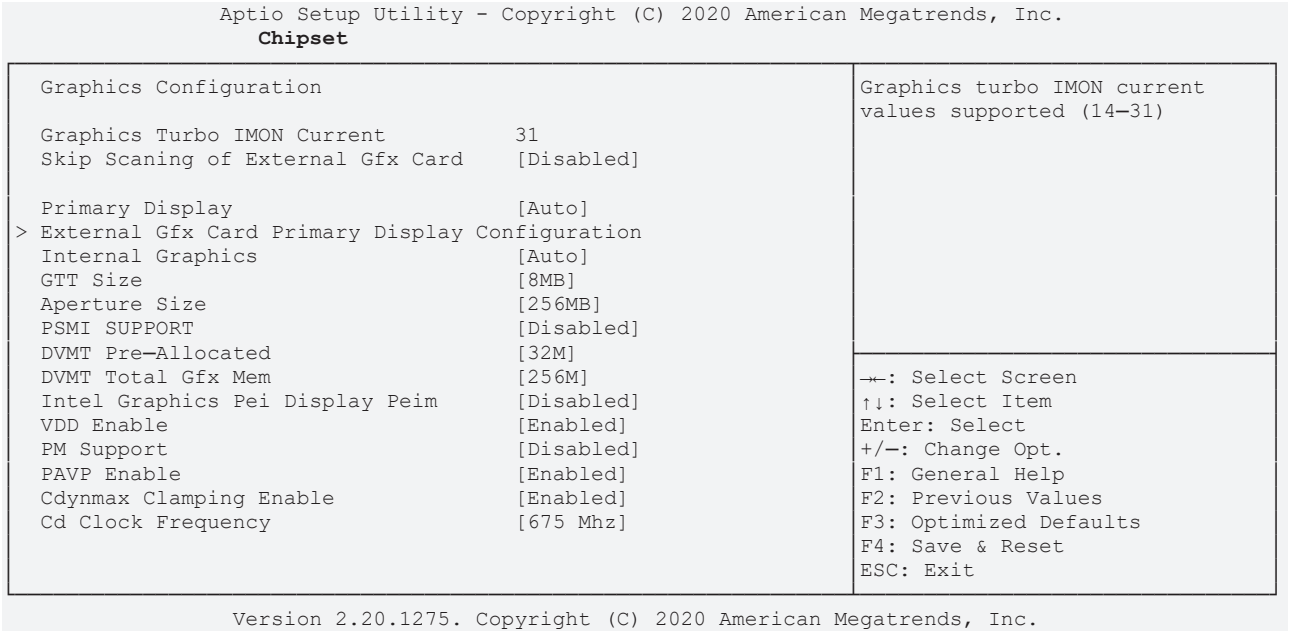
Bios entry	Options
System Agent (SA) Configuration	Submenu see: System Agent (SA) Configuration [▶ 80]
PCH-IO Configuration	Submenu see: PCH-IO Configuration [▶ 82]

6.4.1 System Agent (SA) Configuration



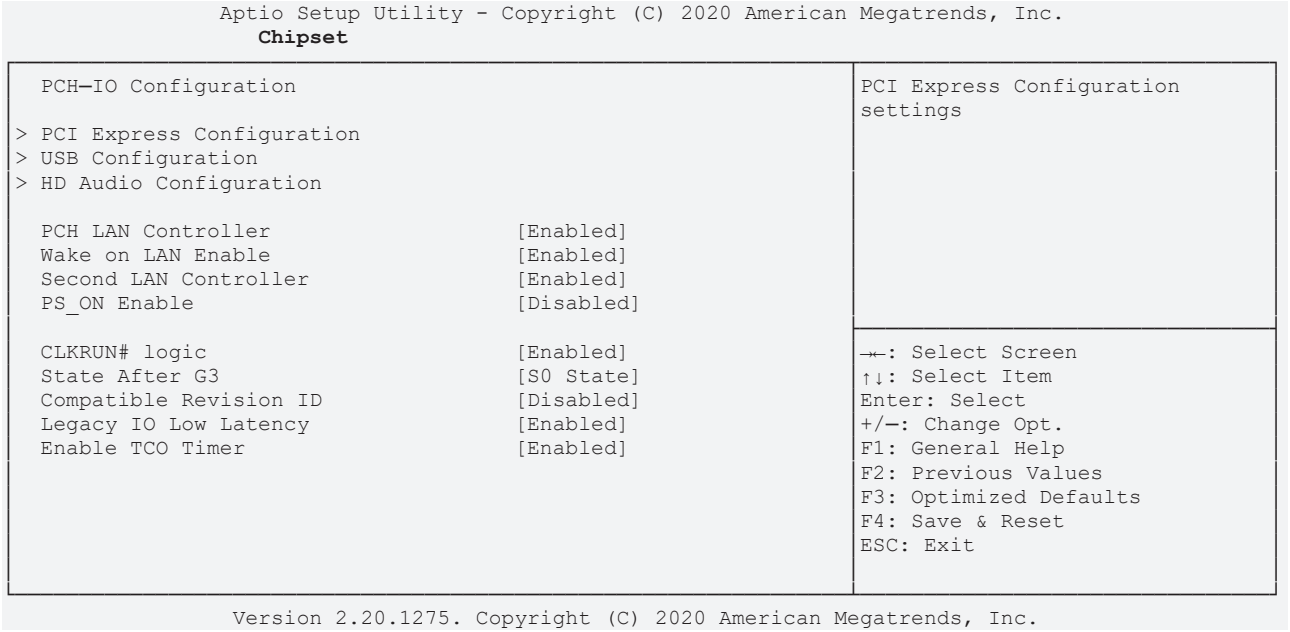
Bios entry	Options
System Agent (SA) Configuration	
SA PCIe code version	None
VT-d	None
Graphics Configuration	Submenu see: Graphics Configuration [▶ 81]
Stop grant configuration	Auto/Manual
VT-d	Enabled/Disabled
CHAP device (B0:07:F0)	Disabled/Enabled
Thermal device (B0:D4:F0)	Enabled/Disabled
GNA device (B0:D8:F0)	Enabled/Disabled
CRID support	Disabled/Enabled
Above 4GB MMIO BIOS assignment	Disabled/Enabled
X2APIC Opt Out	Disabled/Enabled
IPU device (B0:D5:F0)	Disabled/Enabled

6.4.1.1 Graphics Configuration



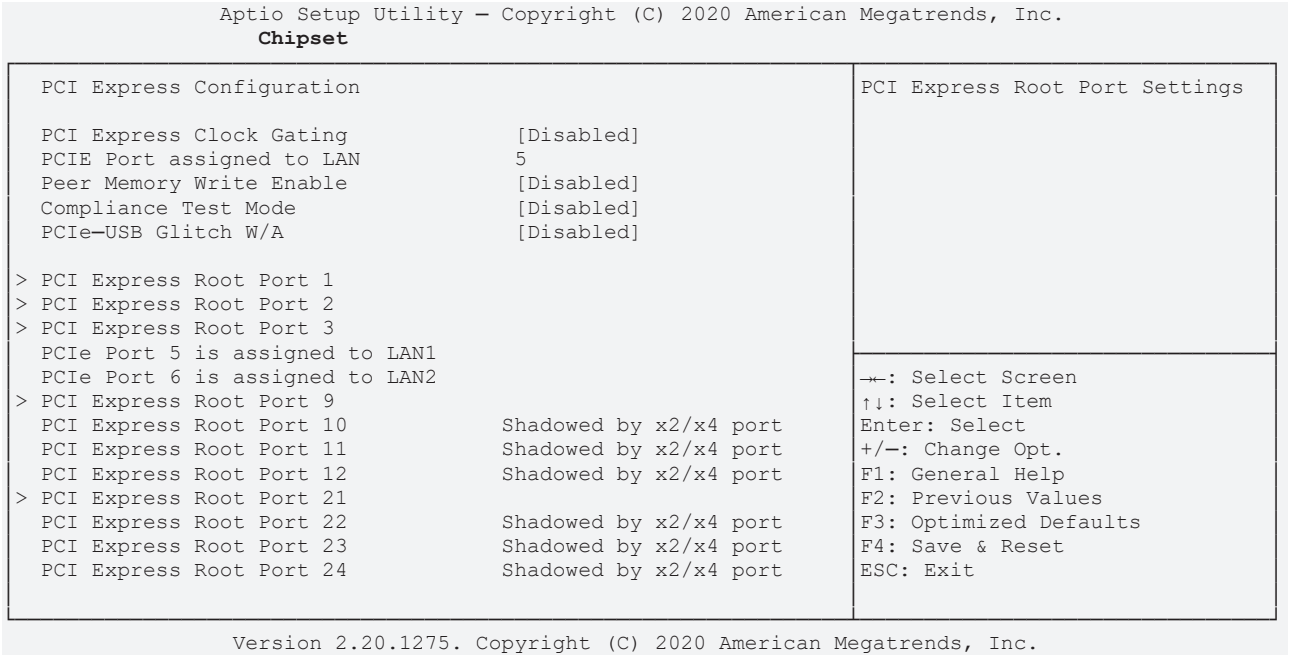
Bios entry	Options
Graphics Configuration	
Graphics Turbo IMON Current	None
Skip Scanning of External Gfx Card	Disabled/Enabled
Primary Display	Auto/IGFX/PCI/SG
External Gfx Card Primary Display Configuration	None
Internal Graphics	Auto/Disabled/Enabled
GTT Size	2/4/8 MB
Aperture Size	128/256/512/1024/2048 MB
PSMI SUPPORT	Disabled/Enabled
DVMT Pre-Allocated	0M, 32M…60M
DVMT Total Gfx Mem	128M/256M/MAX
Intel Graphics Pei Display Peim	Disabled/Enabled
VDD Enable	Enabled/Disabled
PM Support	None
PAVP Enable	Enabled/Disabled
Cdynmax Clamping Enable	Enabled/Disabled
Cd Clock Frequency	337.5/450/540/675 Mhz

6.4.2 PCH-IO Configuration



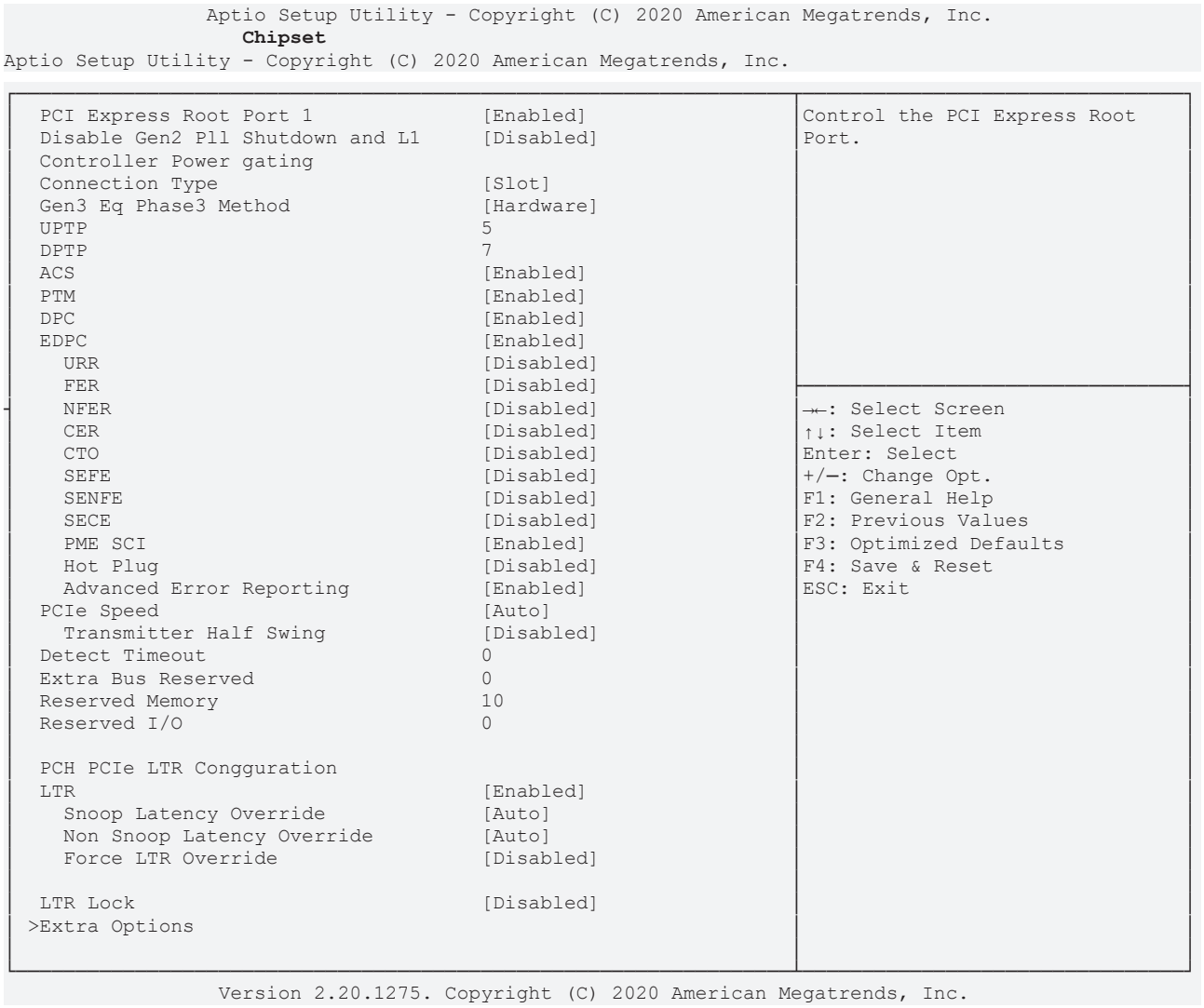
Bios entry	Options
PCH-IO Configuration	
PCI Express Configuration	Submenu see: PCI Express Configuration (Q370) [▶ 83]
USB Configuration	Submenu see: USB Configuration [▶ 87]
HD Audio Configuration	Submenu see: HD Audio Configuration [▶ 87]
PCH LAN controller	Enabled/Disabled
Wake on LAN Enable	Enabled/Disabled
Second LAN controller	Enabled/Disabled
PS_ON Enable	Disabled/Enabled
CLKRUN# logic	Enabled/Disabled
State after G3	S0 state/S5 state
Compatible revision ID	None
Legacy IO low latency	Enabled/Disabled
Enable TCO timer	Disabled/Enabled

6.4.2.1 PCI Express Configuration (Q370)



Bios entry	Options
PCI Express Configuration	
PCI Express Clock Gating	Disabled/Enabled
PCIE port assigned to LAN	None
Peer Memory Write Enable	Disabled/Enabled
Compliance Test Mode	Disabled/Enabled
PCIe USB Glitch W/A	Disabled/Enabled
PCI Express Root Port 1	See submenu: PCI Express Root Port 1 [▶ 84]
PCI Express Root Port 2	See submenu: PCI Express Root Port 1 [▶ 84]
PCI Express Root Port 3	See submenu: PCI Express Root Port 1 [▶ 84]
PCIe Port 5 is assigned to LAN1	None
PCIe Port 6 is assigned to LAN2	None
PCI Express Root Port 9	See submenu: PCI Express Root Port 1 [▶ 84]
PCI Express Root Port 10	None
PCI Express Root Port 11	None
PCI Express Root Port 12	None
PCI Express Root Port 21	See submenu: PCI Express Root Port 1 [▶ 84]
PCI Express Root Port 22	None
PCI Express Root Port 23	None
PCI Express Root Port 24	None

6.4.2.1.1 PCI Express Root Port 1



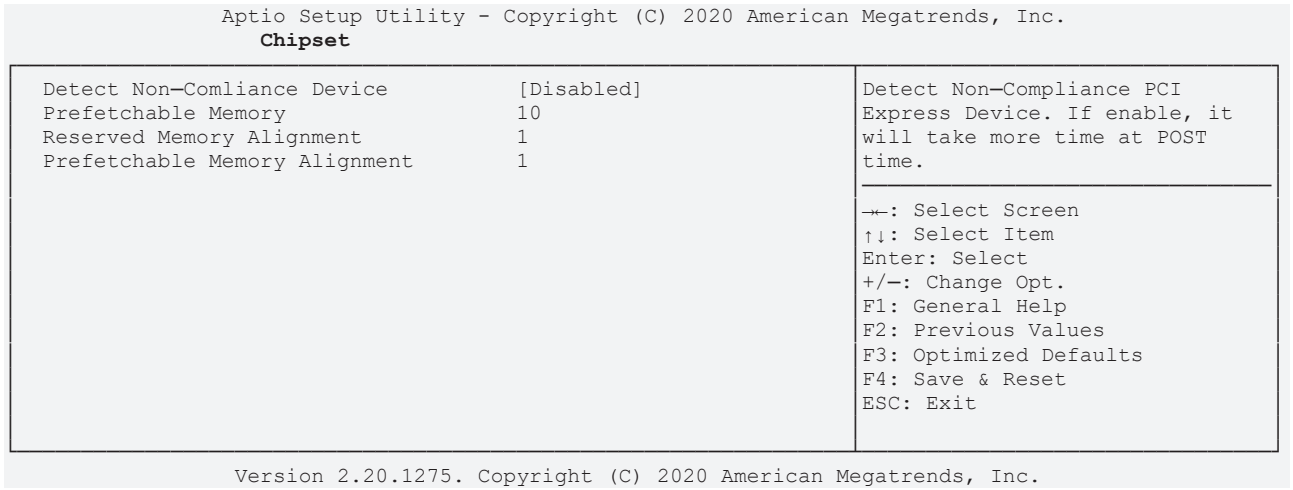
BIOS entry	Options
PCI Express Root Port 1	Disabled/Enabled
Disable Gen2 Pll Shutdown and L1 and Controller Power gating	Disabled/Enabled
Connection type	Built-in/Slot
Gen3 Eq Phase3 Method	Hardware/Static Coeff.
UPTP	None
DPTP	None
ACS	Enabled/Disabled
PTM	Enabled/Disabled
DPC	Enabled/Disabled
EDPC	Enabled/Disabled
URR	Disabled/Enabled
FER	Disabled/Enabled
NFER	Disabled/Enabled
CER	Disabled/Enabled
CTO	Disabled/Enabled
SEFE	Disabled/Enabled
SENFE	Disabled/Enabled
PME SCI	Enabled/Disabled
Hot Plug	Disabled/Enabled
Advanced Error Reporting	Enabled/Disabled
PCIe Speed	Auto/Gen1/Gen2/Gen3
Transmitter Half Swing	Disabled/Enabled
Detect Timeout	None
Extra Bus Reserved	None
Reserved Memory	None
Reserved I/O	None
PCH PCIe LTR Configuration	
LTR	Enabled/Disabled
Snoop Latency Override	Disabled/Manual/Auto
Non Snoop Latency Override	Disabled/Manual/Auto
Force LTR Override	Disabled/Enabled
LTR Lock	Disabled/Enabled
Extra Options	Submenu see: Extra Options [▶ 86]

NOTE

PCI Express Configuration

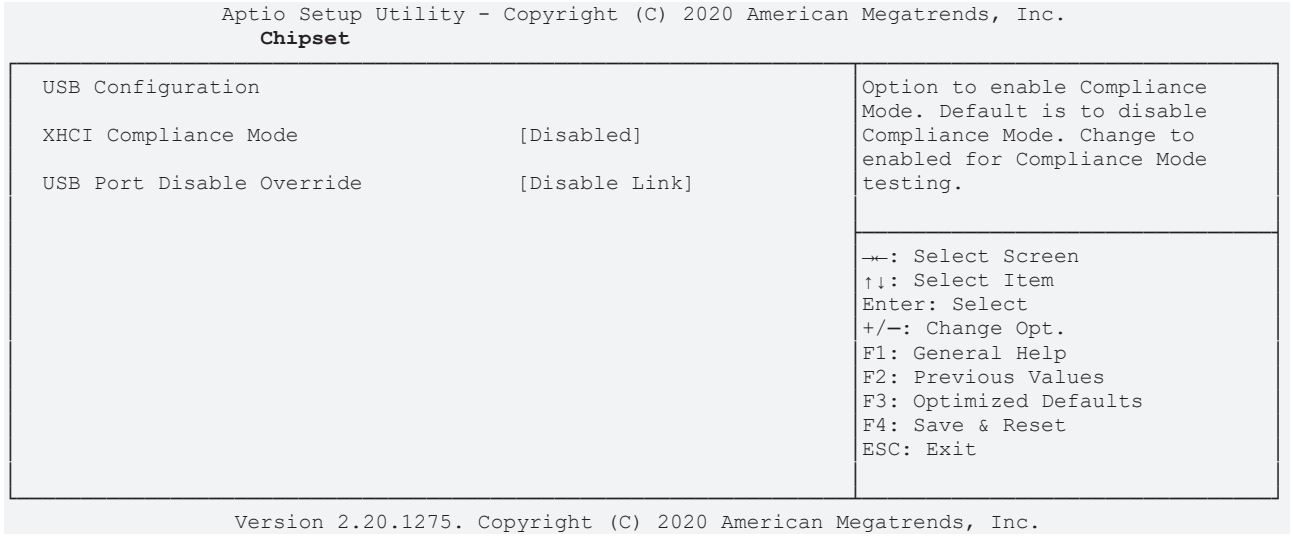
The BIOS entries and options on ports 1-3, 9 and 21 are identical. Port 1 is shown as an example

6.4.2.1.1.1 Extra Options



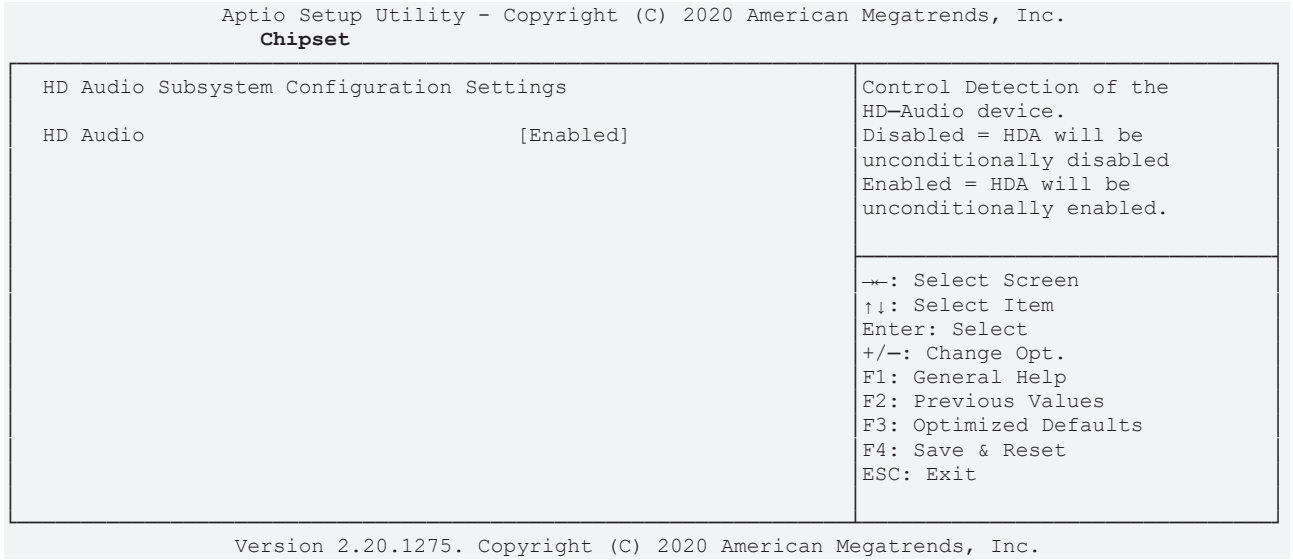
BIOS entry	Options
Detect non-compliance device	Disabled/Enabled
Prefetchable Memory	None
Reserved Memory Alignment	None
Prefetchable Memory Alignment	None

6.4.2.2 USB Configuration



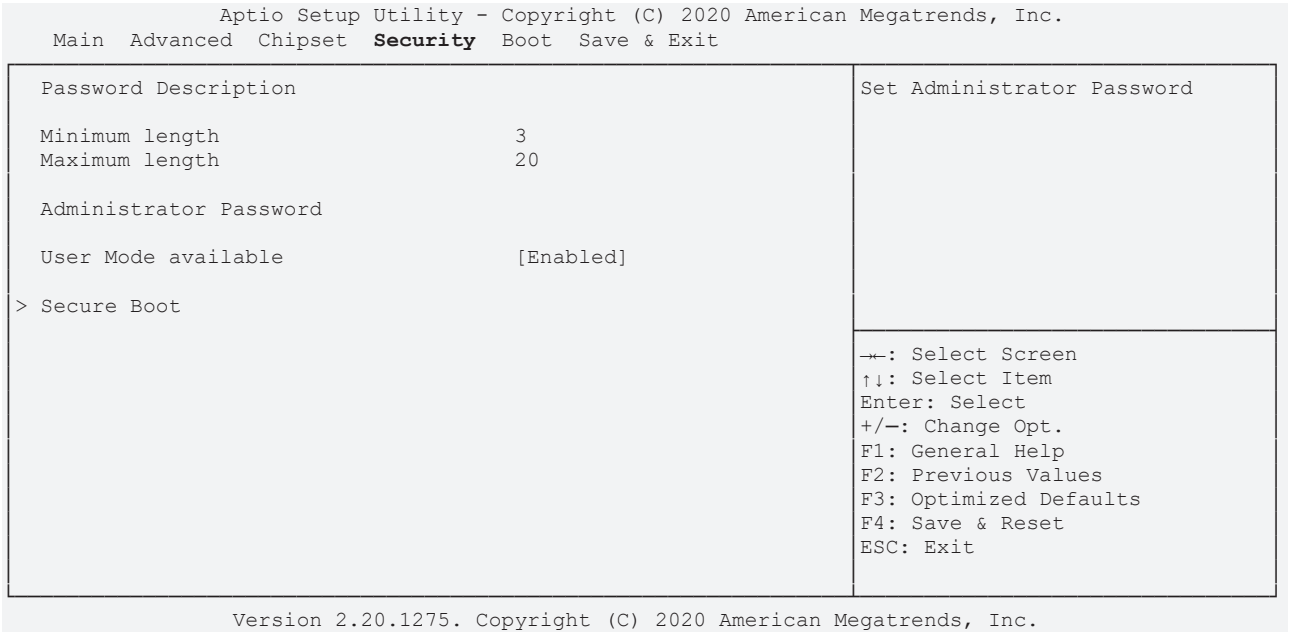
BIOS entry	Options
USB Configuration	
XHCI compliance mode	Disabled/Enabled
USB port disable override	Disable Link/Select Per-Pin

6.4.2.3 HD Audio Configuration



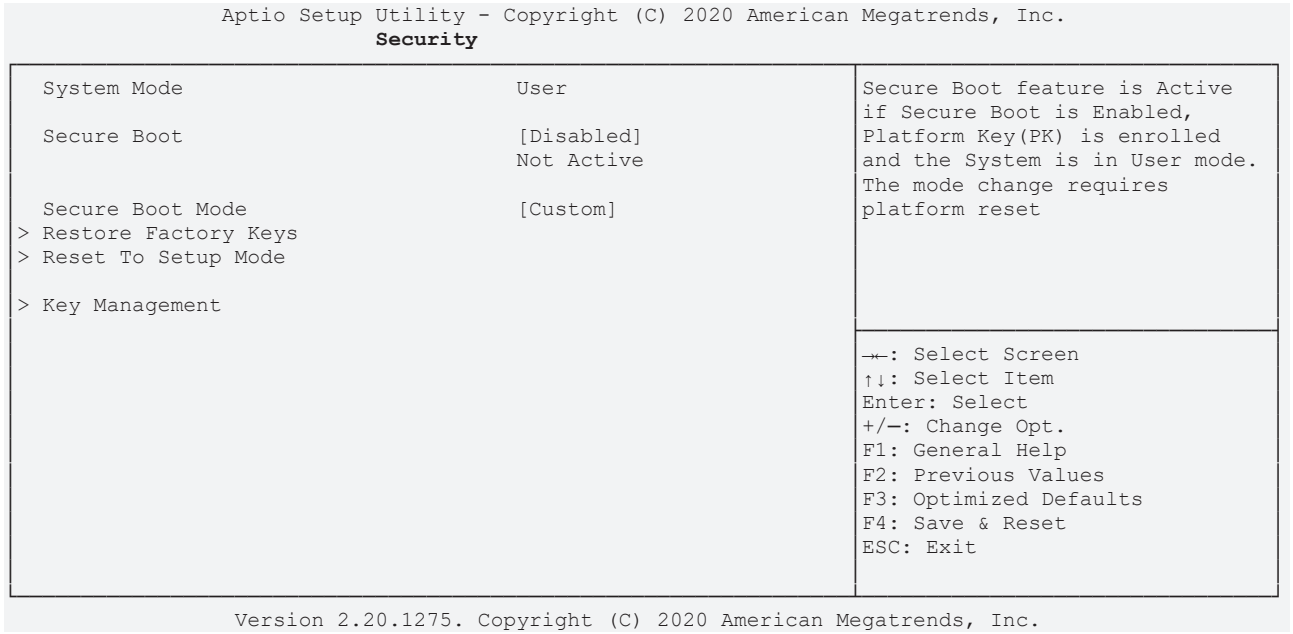
Bios entry	Options
HD audio subsystem configuration settings	
HD audio	Enabled/Disabled

6.5 Security



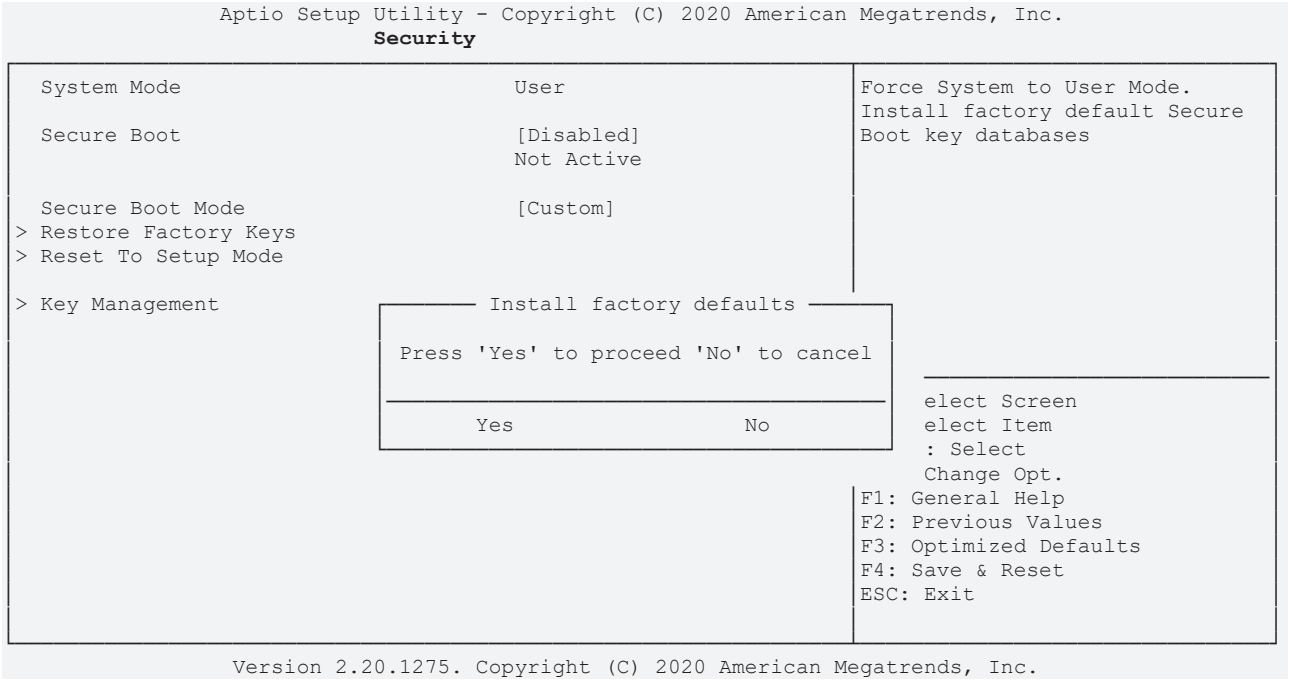
Bios entry	Options
Password Description	
Minimum length	None
Maximum length	None
Administrator Password	Set here an administrator password.
User mode available	Enabled/Disabled
Secure Boot	Submenu see: Secure Boot [▶ 89]

6.5.1 Secure Boot



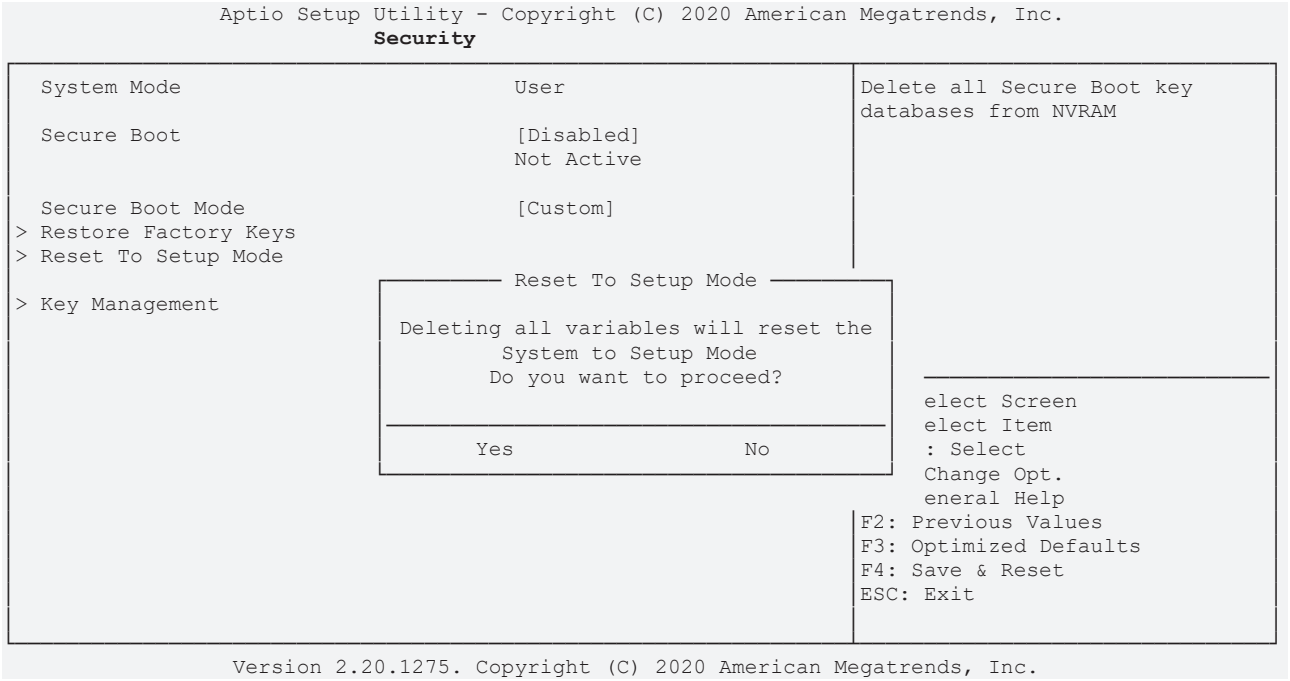
Bios entry	Options
System Mode	None
Secure Boot	Disabled/Enabled Not active
Secure Boot Mode	Custom/Standard
Restore Factory Keys	Submenu see: Restore factory keys [▶ 90]
Reset To Setup Mode	Submenu see: Reset To Setup Mode [▶ 91]
Key Management	Submenu see: Key Management [▶ 92]

6.5.1.1 Restore factory keys



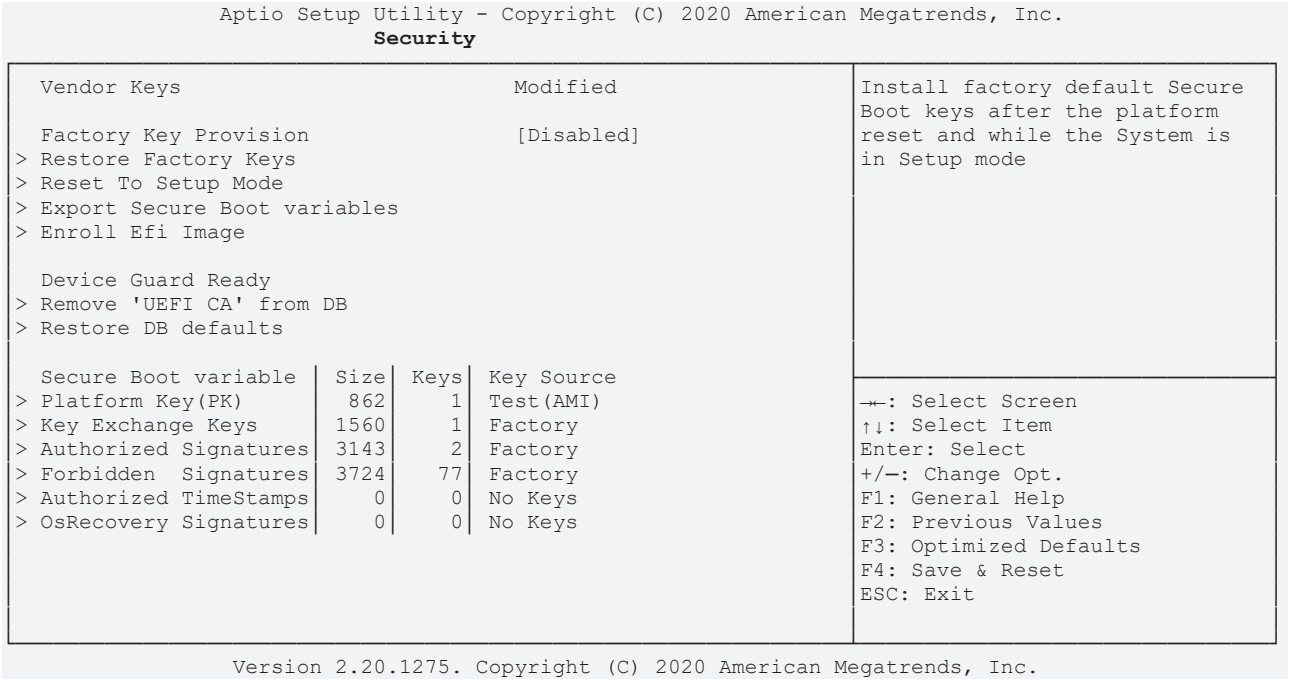
Bios entry	Options
System Mode	None
Secure Boot	Disabled/Enabled
Secure Boot Mode	Custom/Standard
Restore Factory Keys	Install factory defaults, see box

6.5.1.2 Reset To Setup Mode



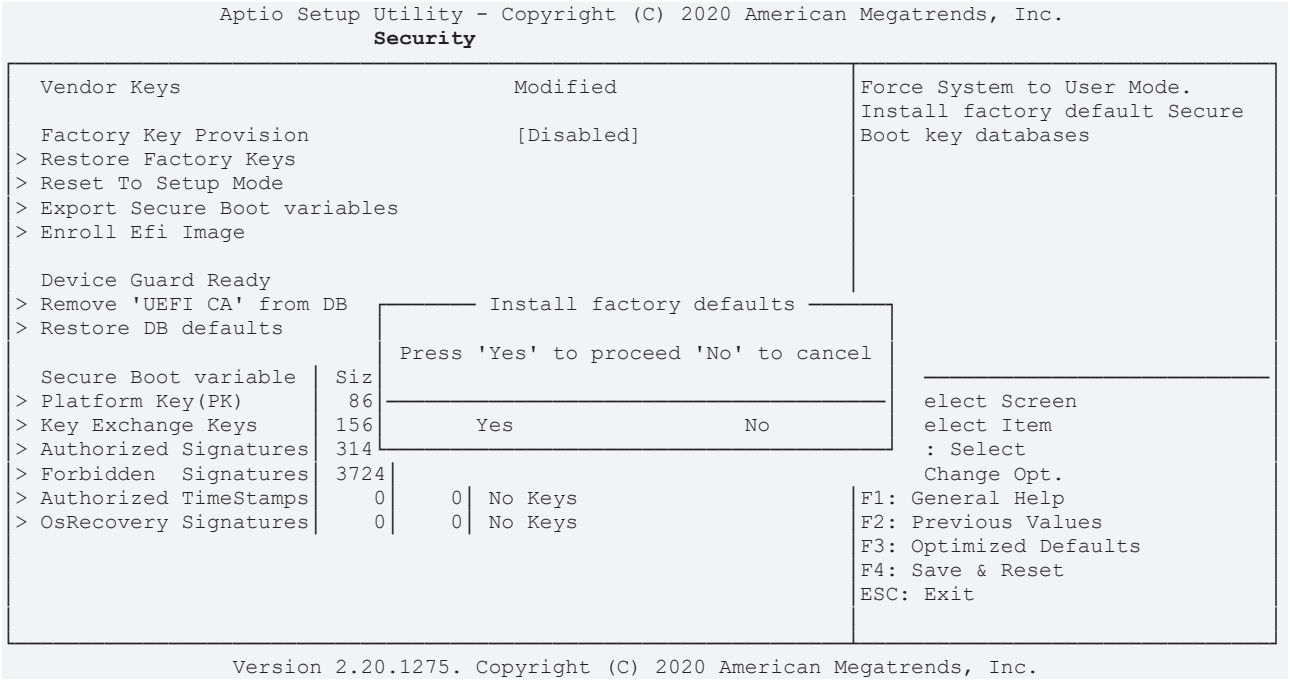
Bios entry	Options
System Mode	none
Secure Boot	Disabled/Enabled Not active
Secure Boot Mode	Custom/Standard
Reset To Setup Mode	Reset To Setup Mode, see box

6.5.1.3 Key Management



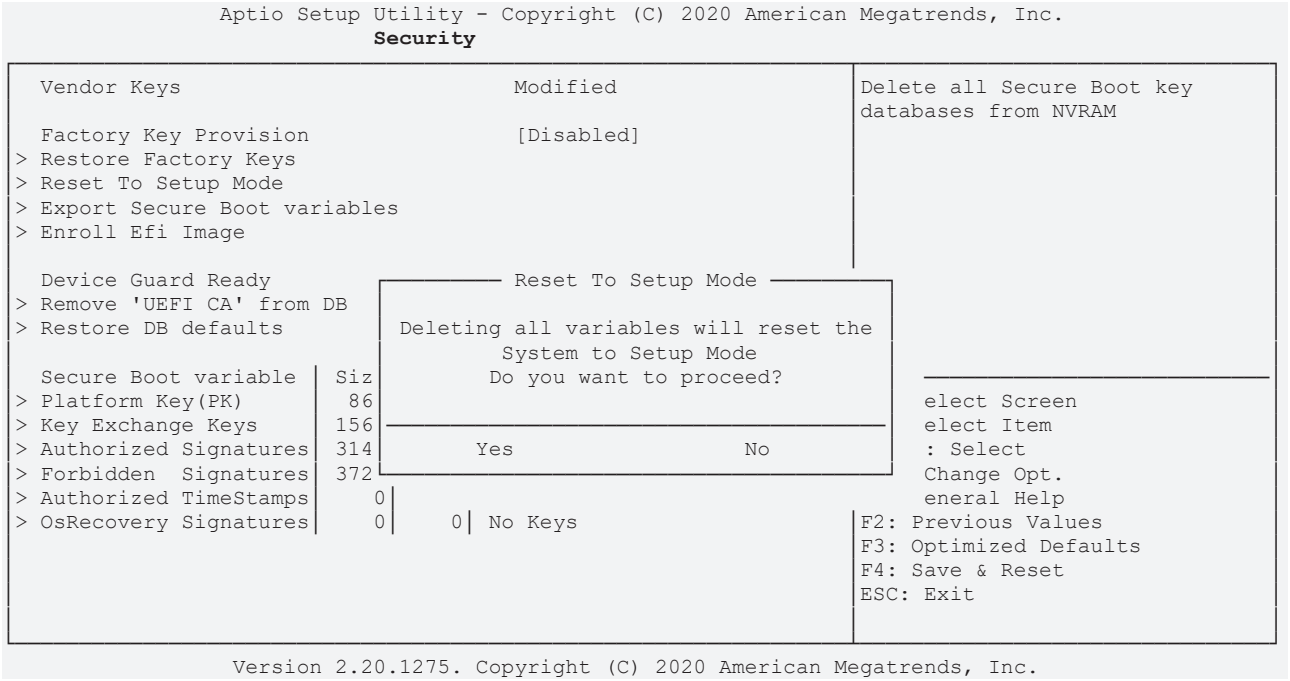
Bios entry	Options
Vendor Keys	None
Factory Key Provision	Disabled/Enabled
Restore Factory Keys	Submenu see: Restore Factory Keys [▶ 93]
Reset To Setup Mode	Submenu see: Reset To Setup Mode [▶ 94]
Export Secure Boot variables	Submenu see: Export Secure Boot Variables [▶ 95]
Enroll Efi Image	Submenu see: Enroll Efi Image [▶ 96]
Device Guard Ready	
Remove 'UEFI CA' from DB	Submenu see: Remove UEFI CA from DB [▶ 97]
Restore DB defaults	Submenu see: Restore DB defaults [▶ 98]
Secure Boot variables	Press enter key
PlatformKey(PK)	Press enter key
Key Exchange Keys	Press enter key
Authorized Signatures	Press enter key
Forbidden Signatures	Press enter key
Authorized TimeStamps	Press enter key
OsRecovery Signatures	Press enter key

6.5.1.3.1 Restore Factory Keys



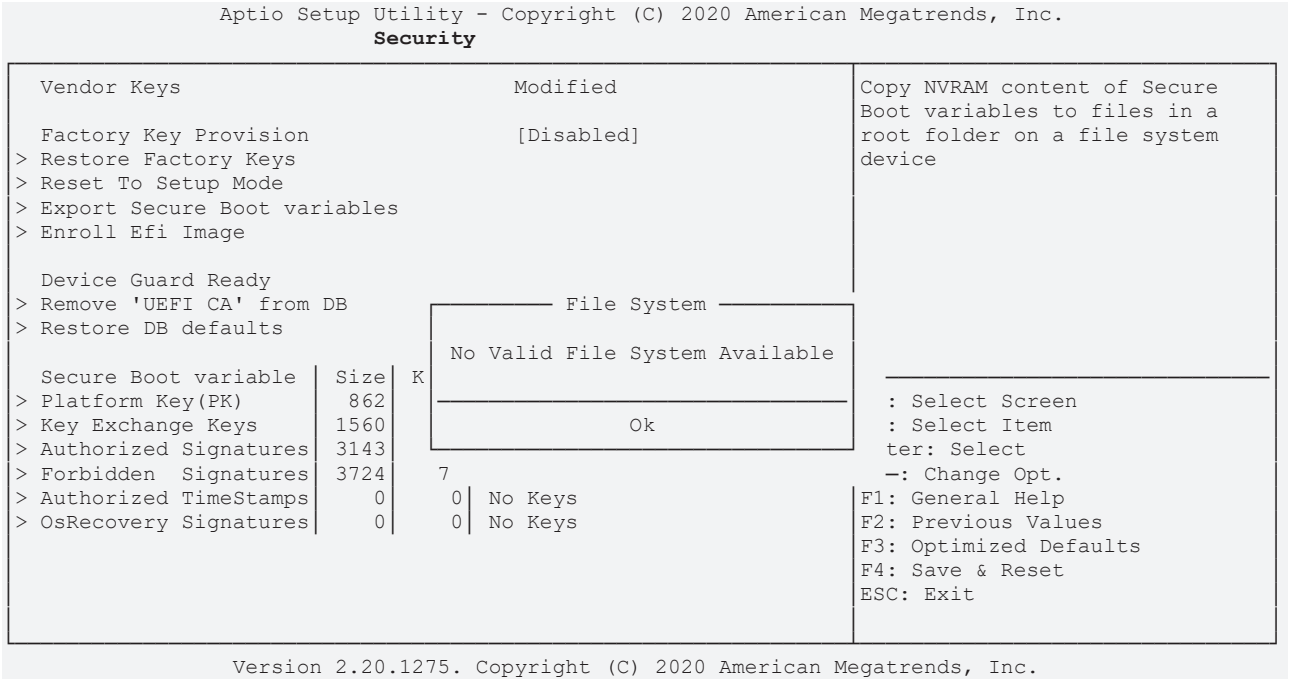
Bios entry	Options
Vendor Keys	None
Restore Factory Keys	Install factory defaults, see box

6.5.1.3.2 Reset To Setup Mode



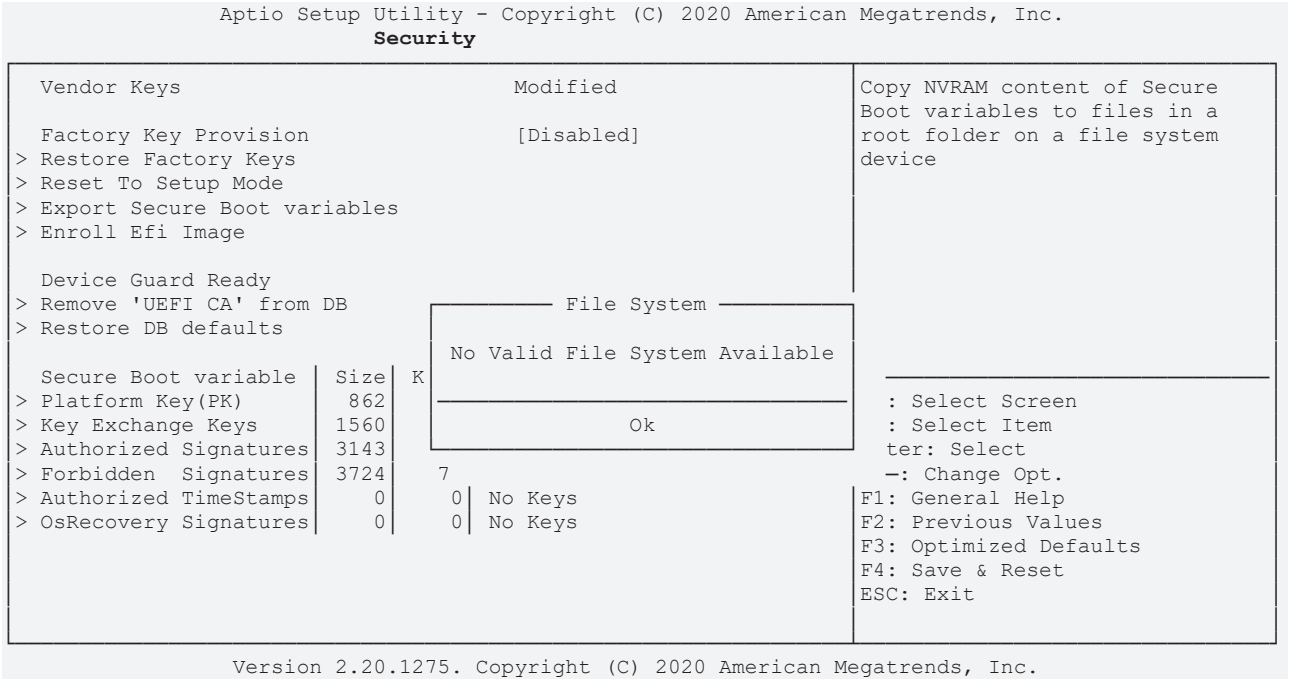
Bios entry	Options
Vendor Keys	None
Reset To Setup Mode	Reset To Setup Mode, see box

6.5.1.3.3 Export Secure Boot Variables



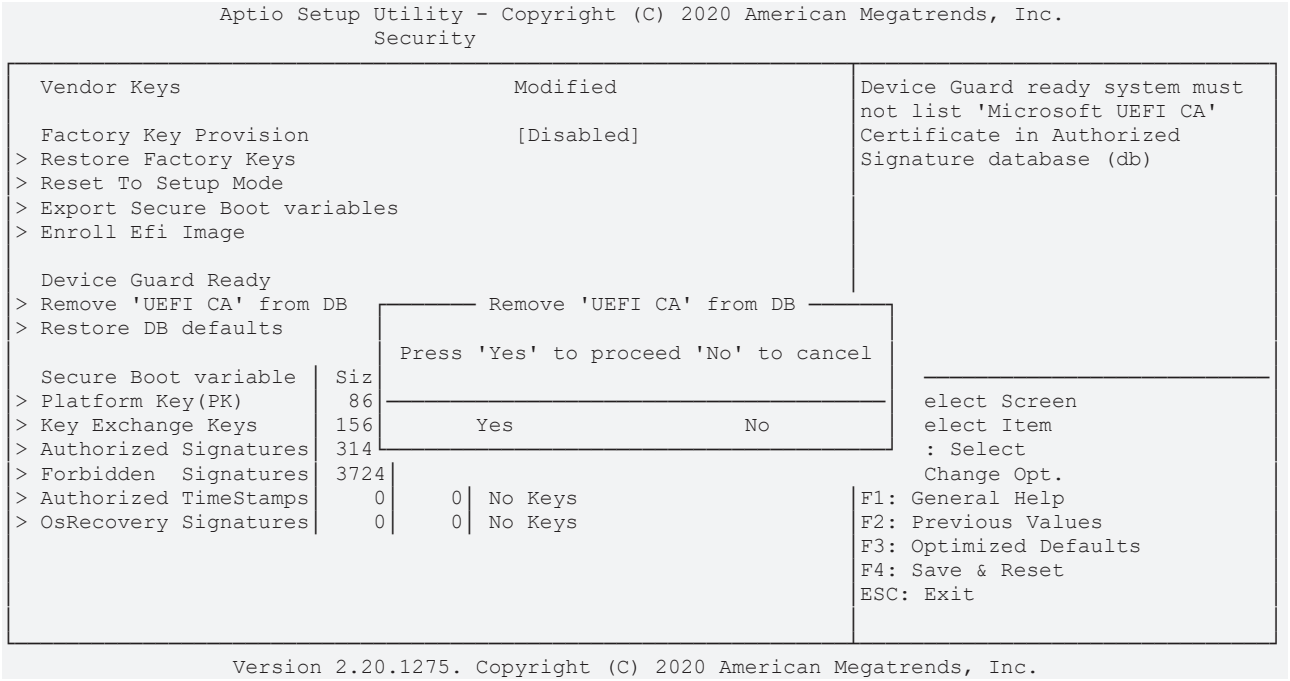
Bios entry	Options
Vendor Keys	None
Export Secure Boot variables	File System, see box

6.5.1.3.4 Enroll Efi Image



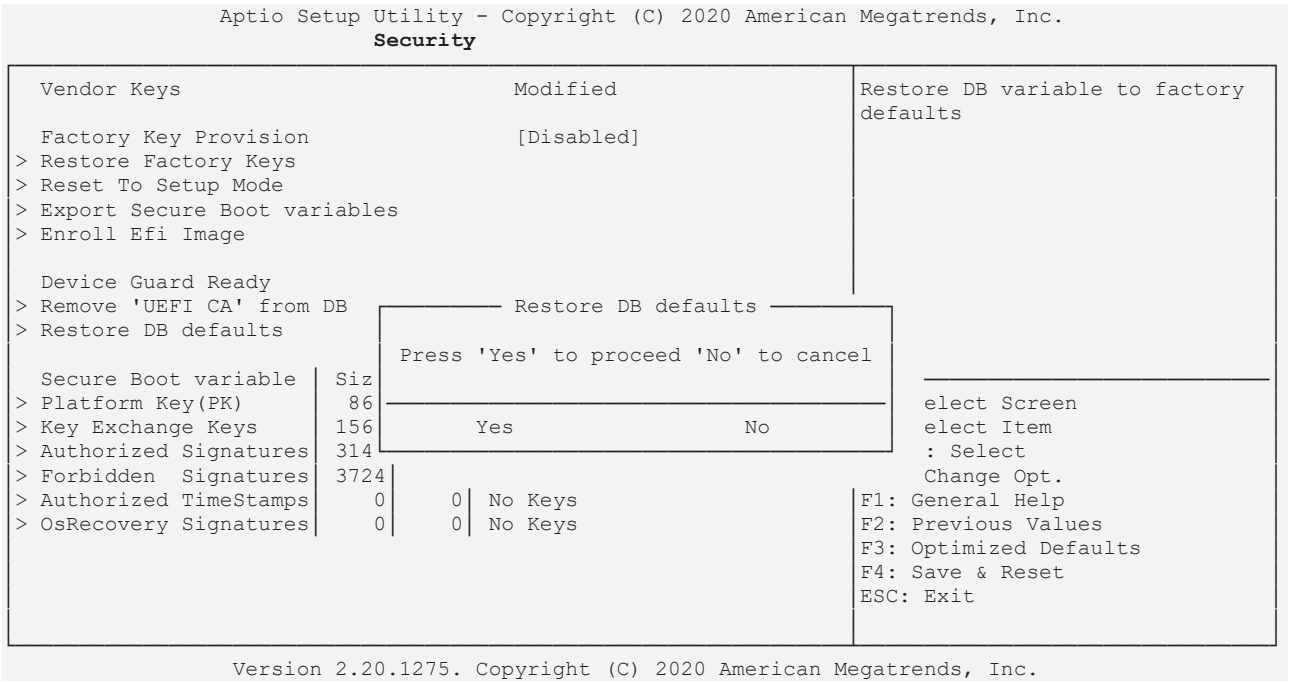
Bios entry	Options
Vendor Keys	None
Enroll Efi Image	File System, see box

6.5.1.3.5 Remove UEFI CA from DB



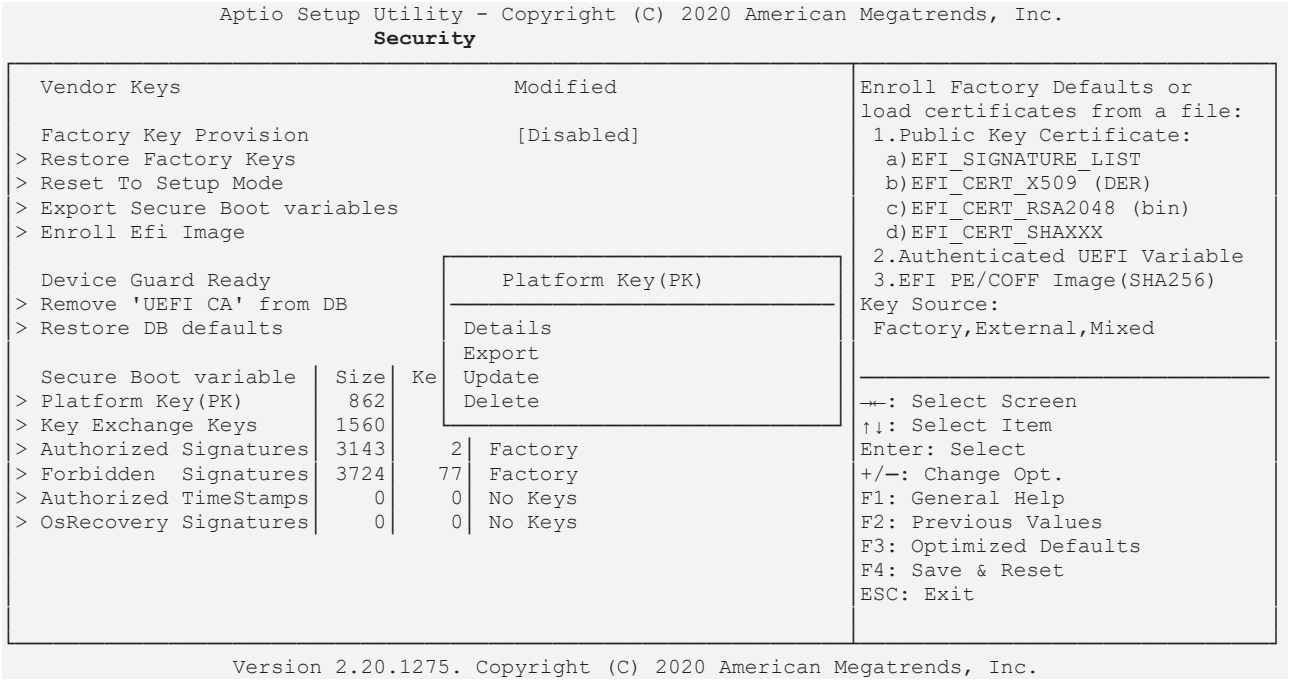
Bios entry	Options
Vendor Keys	None
Remove ‘UEFI CA’ from DB	Remove ‘UEFI CA‘ from DB, see box

6.5.1.3.6 Restore DB defaults



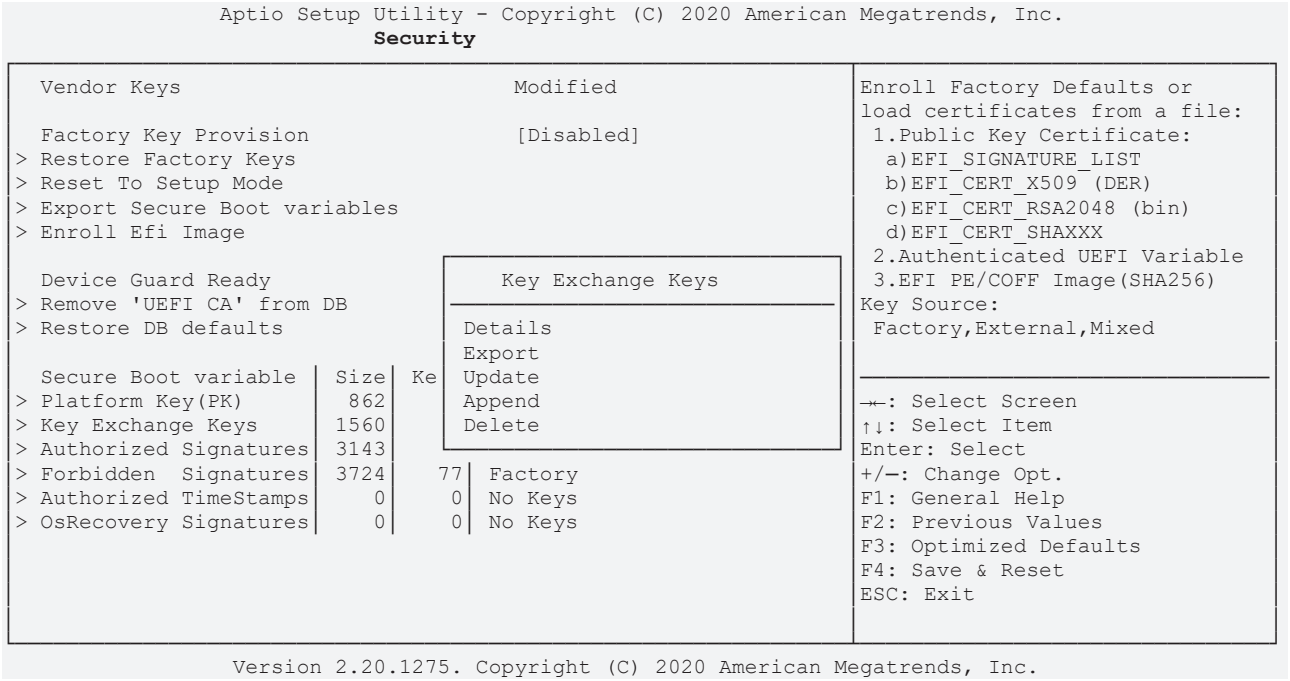
Bios entry	Options
Vendor Keys	None
Restore DB defaults	Restore DB defaults, see box

6.5.1.3.7 Platform Key (PK)



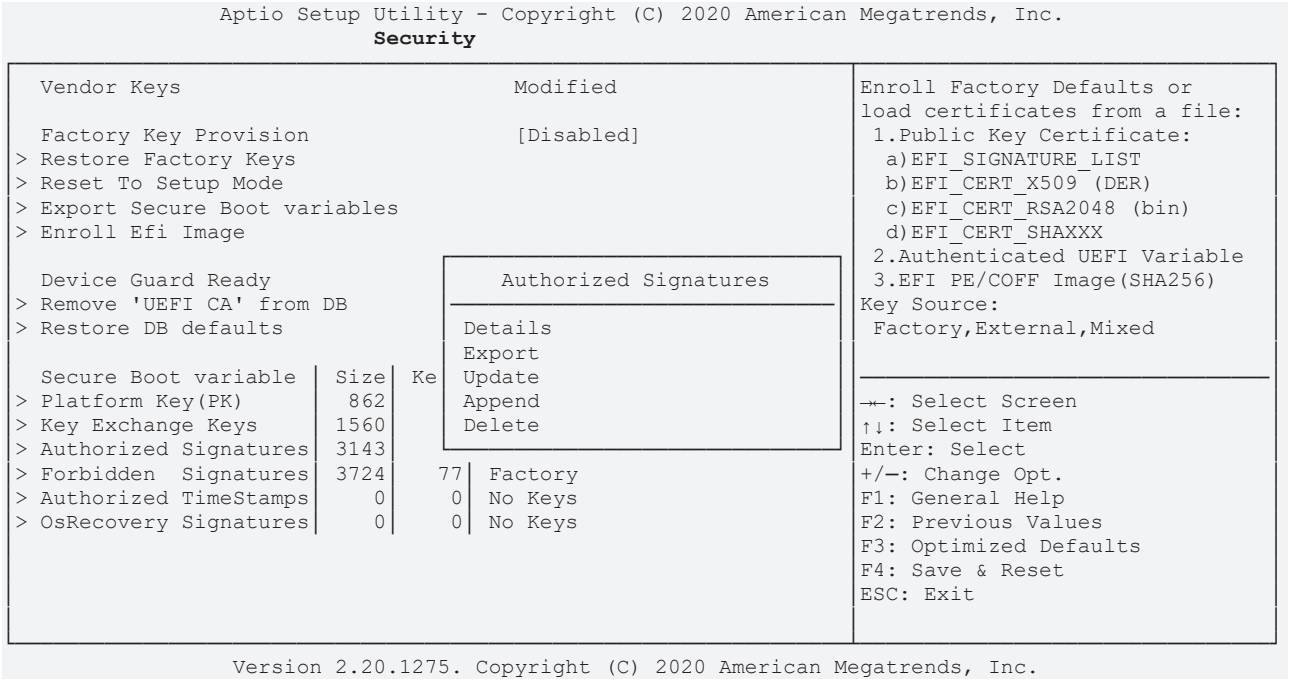
Bios entry	Options
Vendor Keys	None
Platform Key (PK)	Platform Key (PK), see box

6.5.1.3.8 Key Exchange Keys



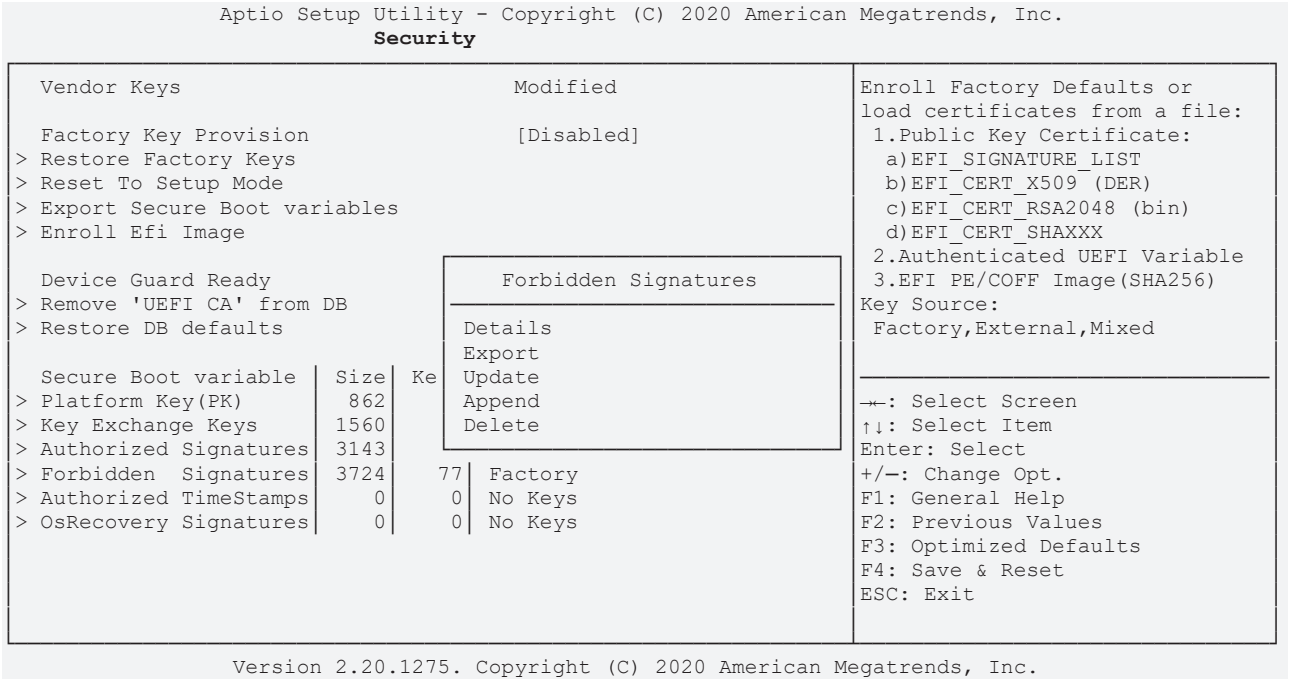
Bios entry	Options
Vendor Keys	None
Key Exchange Keys	Key Exchange Keys, see box

6.5.1.3.9 Authorized Signatures



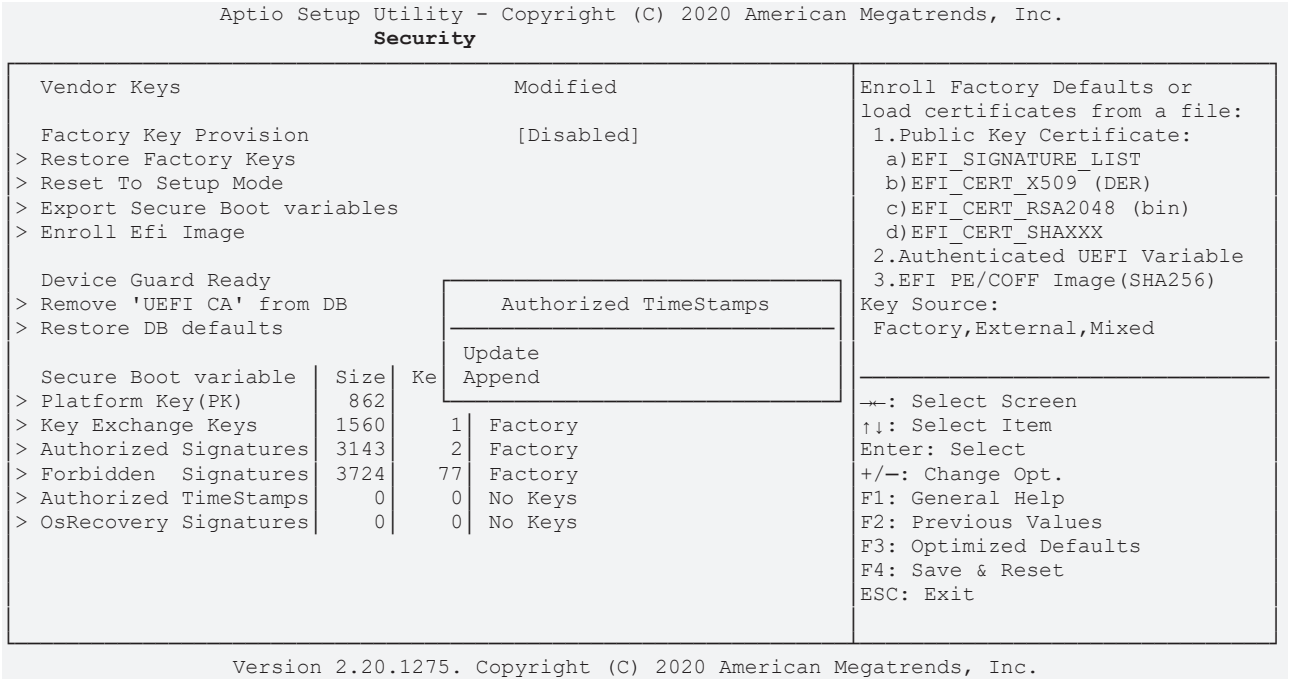
Bios entry	Options
Vendor Keys	None
Authorized Signatures	Authorized Signatures, see box

6.5.1.3.10 Forbidden Signatures



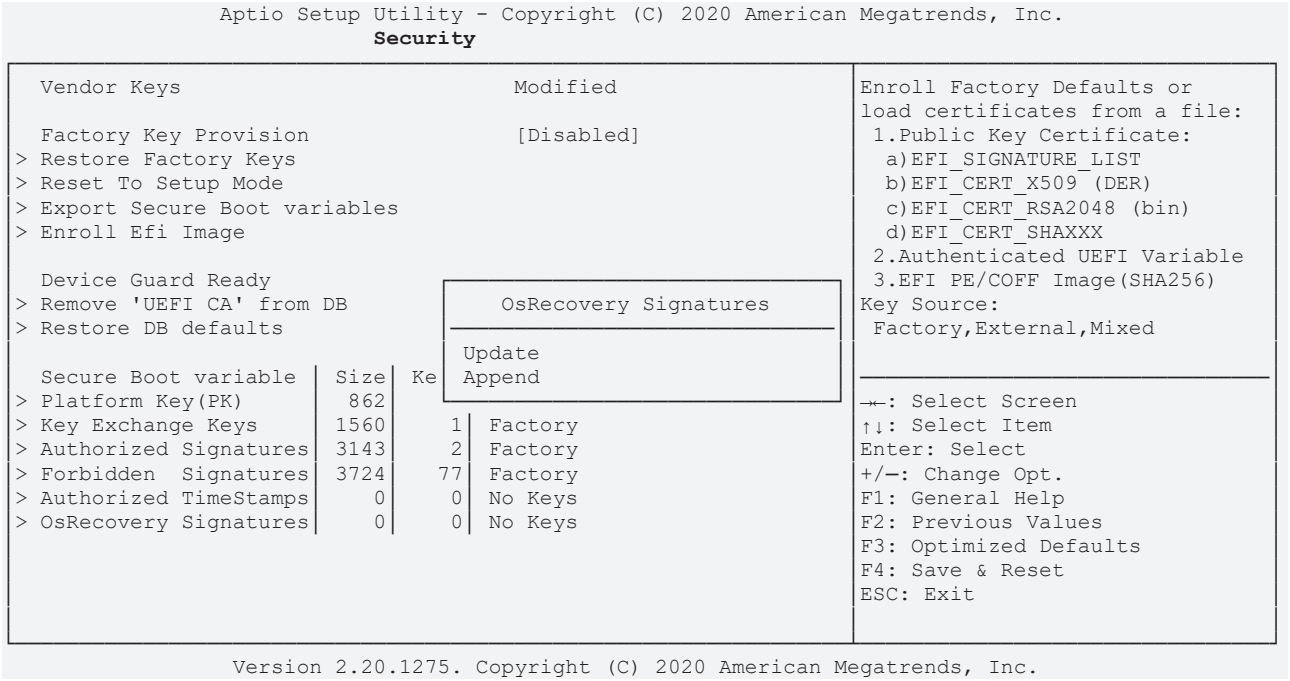
Bios entry	Options
Vendor Keys	None
Forbidden Signatures	Forbidden Signatures, see box

6.5.1.3.11 Authorized TimeStamps



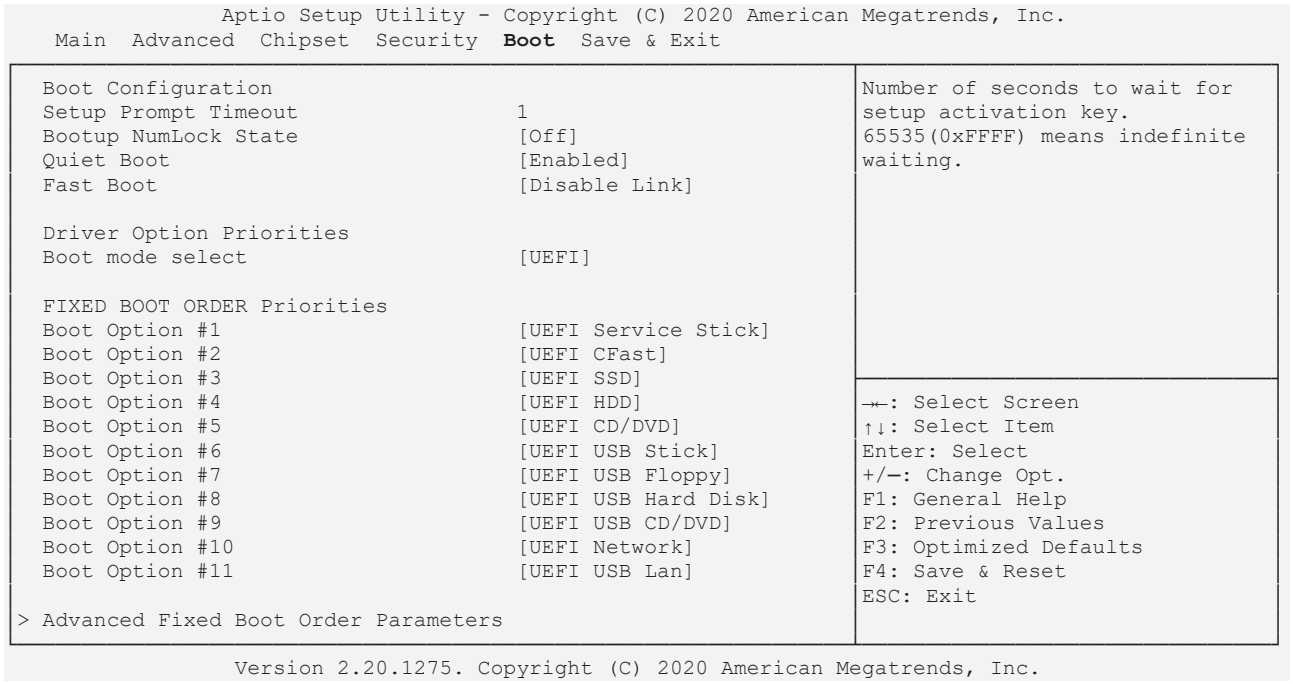
Bios entry	Options
Vendor Keys	None
Authorized TimeStamps	Authorized TimeStamps, see box

6.5.1.3.12 OsRecovery Signatures



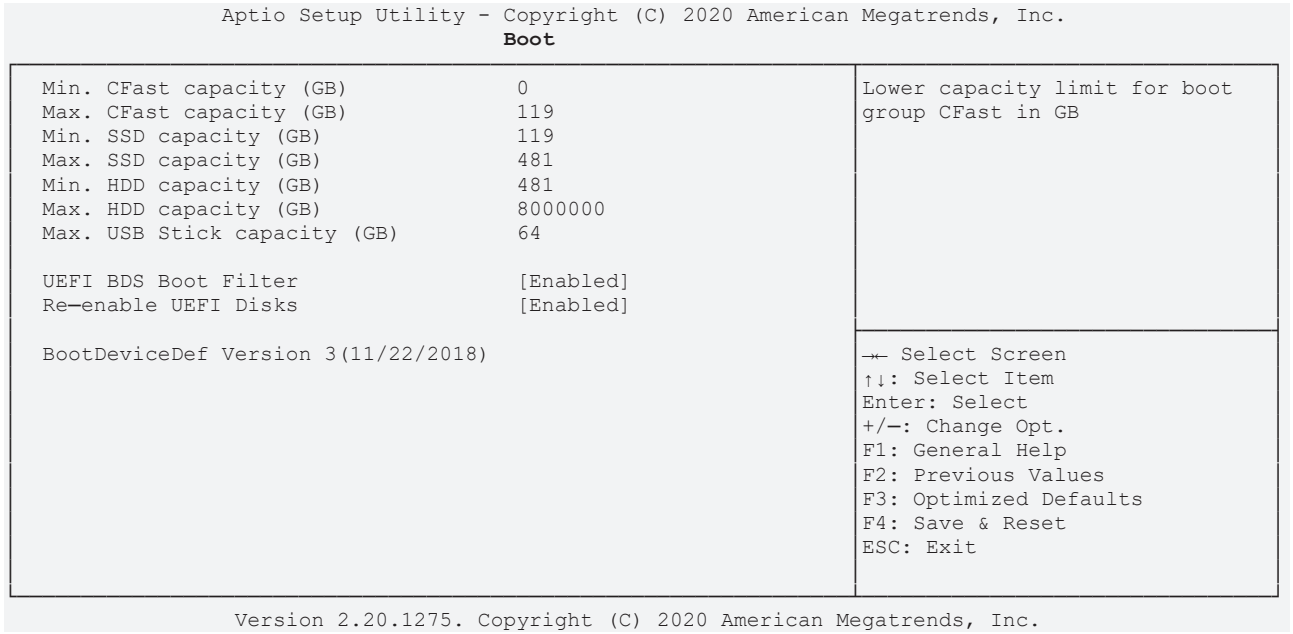
Bios entry	Options
Vendor Keys	None
OsRecovery Signatures	OsRecovery Signatures, see box

6.6 Boot



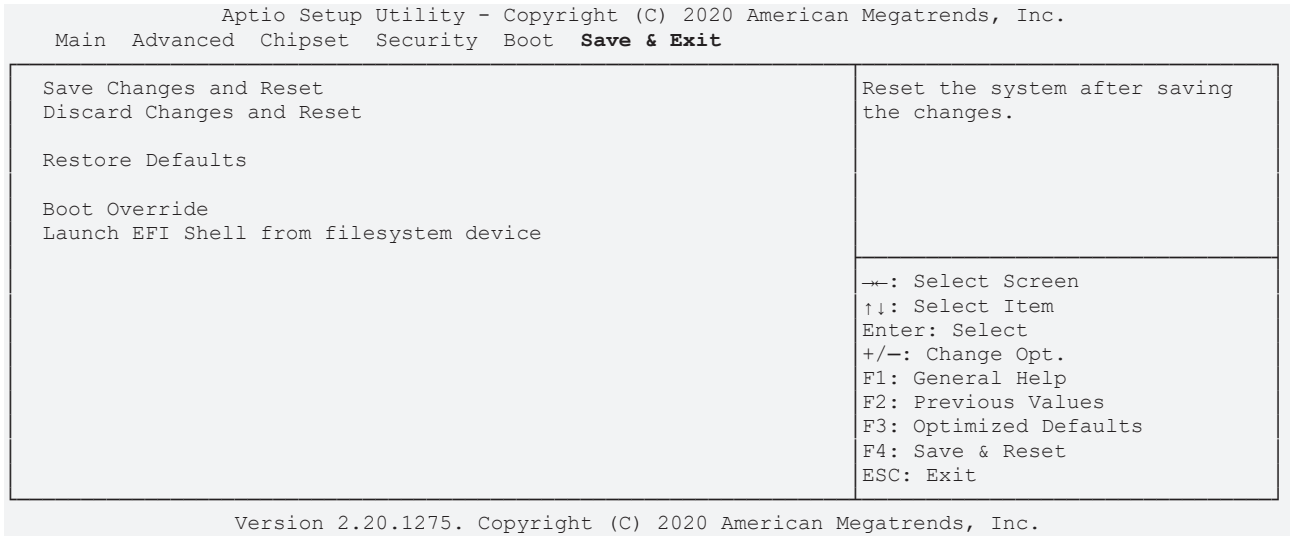
Bios entry	Options
Boot Configuration	
Setup Prompt Timeout	1
Bootup NumLok state	On/Off
F7 Boot Menu	Enabled/Disabled
Quiet Boot	Enabled/Disabled
Fast boot	Disable Link/Enabled
Boot mode select	None
Fixed Boot Order Priorities	
Boot Option #1-11	Here you can set the order of the boot media to be used.
Advanced Fixed Boot Order Parameters	Submenu see: Advanced Fixed Boot Order Parameters [▶ 106]

6.6.1 Advanced Fixed Boot Order Parameters



Bios entry	Options
Min. CFast capacity (GB)	None
Max. CFast capacity (GB)	None
Min. SSD capacity (GB)	None
Max. SSD capacity (GB)	None
Min. HDD capacity (GB)	None
Max. HDD capacity (GB)	None
Max. USB Stick capacity (GB)	None
UEFI BDS Boot filter	Enabled/Disabled
Re-enable UEFI disks	Enabled/Disabled
BootDeviceDef Version 3(11/22/2018	

6.7 Save & Exit



Bios entry	Options
Save Changes and Reset	
Discard Changes and Reset	Press enter key
Restore Optimized Defaults	Press enter key
Boot Override	
Launch EFI Shell from filesystem device	Press enter key

6.8 BIOS update

The "DecdFlsh" program and a bootable medium with the latest BIOS version are used if the BIOS needs to be updated. When doing this it is important to start the program from a DOS environment without a virtual memory manager such as "EMM386.EXE". If such a memory manager is loaded, the program will abort with an error message or cause a crash.

DecdFlsh is a program for the automatic updating of the BIOS on all boards with AMI-BIOS. All files contained in the zip file must be unpacked into a directory, from where

```
DecdFlsh Bios-Dateiname
```

calling takes place. The name of the BIOS file and its length are checked. The BIOS will now be programmed.

The system must not be interrupted during the flashing process, as otherwise the update will abort and the BIOS on the board will be destroyed. The Flash procedure takes about 75 seconds. The necessary firmware update takes place automatically.

NOTE

Damage due to incorrect update execution

Consequences: if the BIOS update is performed incorrectly, the board can become unusable. Therefore a BIOS update should only be done if the corrections / additions that the new BIOS version brings with it are really needed.

Before a planned BIOS update, it is essential to ensure that the BIOS file to be reloaded is really released for exactly this board and for exactly this board version. If an inappropriate file is used, the board will inevitably not boot afterwards.

7 Mechanical drawing

NOTE

Dimensional notation

All dimensions in mil (1 mil = 0.0254 mm). Data in square brackets are in mm.

7.1 PCB: Dimensions

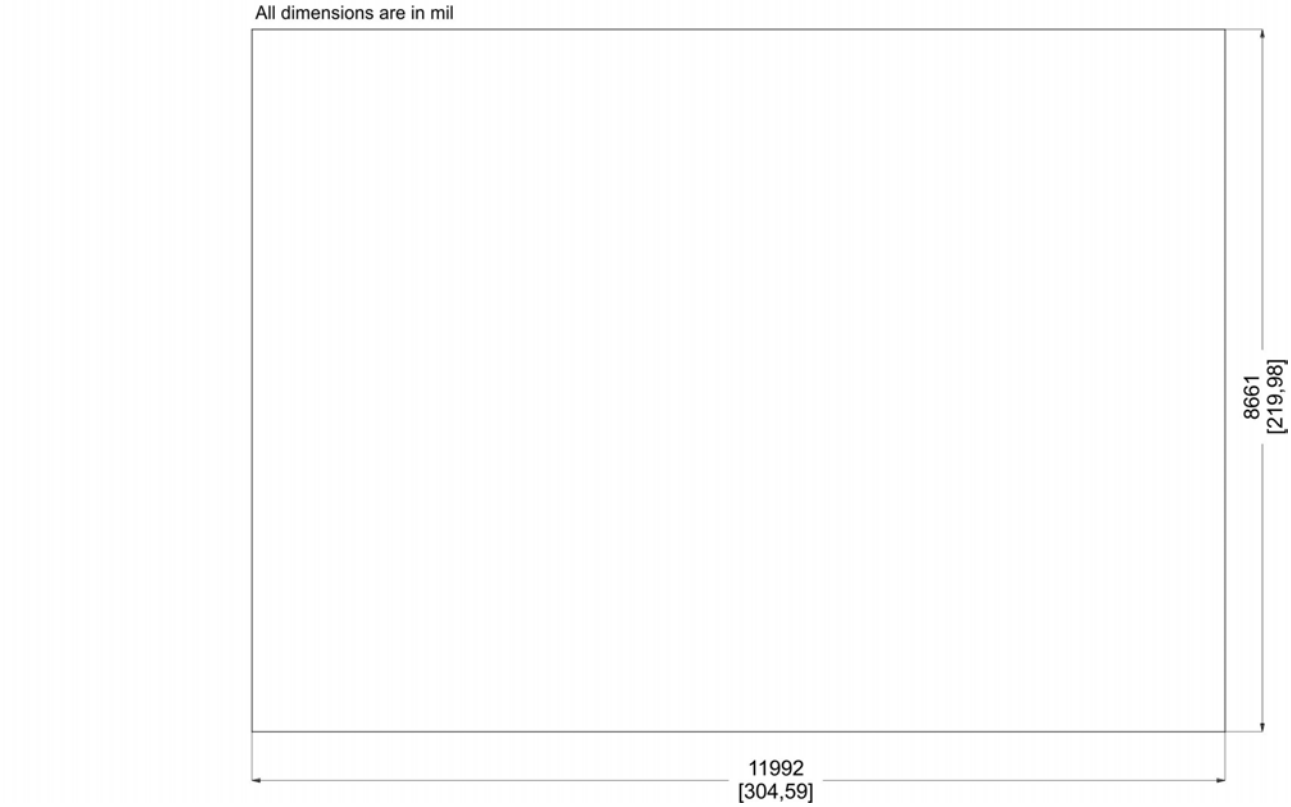


Fig. 29: PCB Outlines

7.2 PCB: Mounting holes

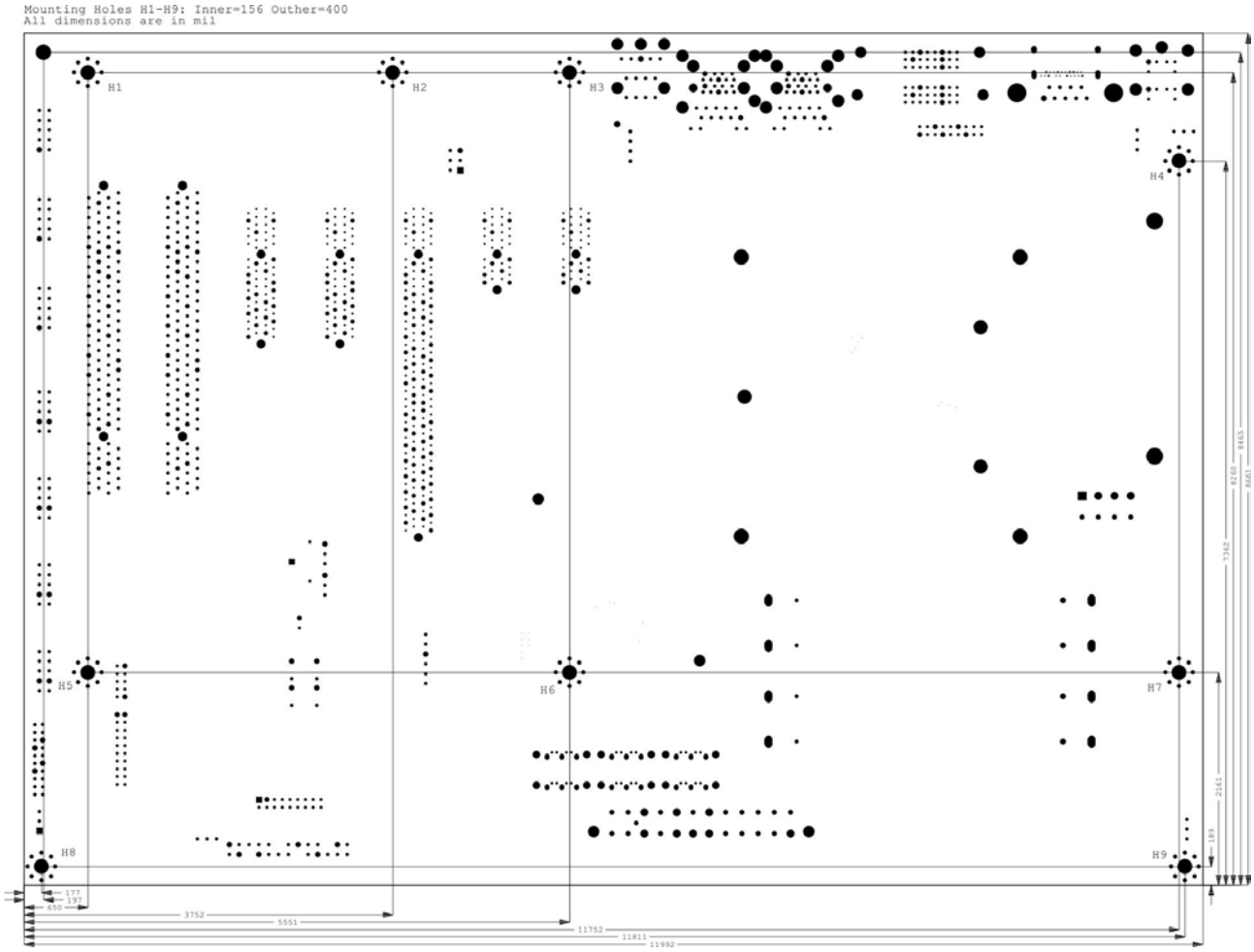


Fig. 30: PCB mounting holes

8 Technical data

8.1 Electrical data

Power supply	
Board	ATX connector incl. 2 x 4-pin connector 12 V (CPU)
RTC	≥3 V

Current consumption	
Board	Typical power consumption under load: 10 W without CPU and expansion cards*
RTC	≤ 10 µA
*Total power consumption depending on the CPU	

8.2 Environmental conditions

Temperature range	
Operating	0 °C to +60 °C (extended temperature range on request)
Storage	-25 °C to +85 °C
Shipping	-25 °C to +85 °C, for packed boards

Temperature changes	
Operating	0.5 °C per minute, 7.5 °C in 30 minutes
Storage	1.0 °C per minute
Shipping	1.0 °C per minute, for packed boards

Relative humidity	
Operating	5% to 85% (non-condensing)
Storage	5% to 95% (non-condensing)
Shipping	5% to 100% (non-condensing), for packed boards

Impact	
Operating	150 m/s², 6 ms
Storage	400 m/s², 6 ms
Shipping	400 m/s², 6 ms, for packed boards

Vibration	
Operating	10 to 58 Hz, 0.075 mm amplitude 58 to 500 Hz, 10 m/s²
Storage	5 to 9 Hz, 3.5 mm amplitude 9 to 500 Hz, 10 m/s²
Shipping	5 to 9 Hz, 3.5 mm amplitude 9 to 500 Hz, 10 m/s², for packed boards

Note on impact and vibration resistance

The specifications for impact and vibration resistance refer only to the motherboard itself without heat sink, memory module, cabling, etc.

8.3 Thermal specifications

The board is specified for an ambient temperature range of 0 °C to +60 °C (extended temperature range on enquiry). In addition, care must be taken that the temperature of the processor die does not exceed 100 °C. To ensure this a suitable cooling concept must be implemented that is oriented to the maximum power consumption of the processor/chipset. It must also be ensured that any existing controllers are included in the cooling concept. The power consumption of these function blocks may be of the same order of magnitude as the power consumption of the processor.

The board is prepared with drill holes for the use of suitable cooling solutions. We have a series of compatible cooling components in our range. Your distributor will be pleased to assist you in selecting suitable solutions.

NOTE

Prevent the maximum die temperature being exceeded!

It is the end customer's responsibility to ensure that the die temperature of the processor does not exceed 100 °C! Continuous overheating can destroy the board!

If the temperature exceeds 100 °C, the ambient temperature needs to be reduced. Ensure sufficient air circulation if necessary.

9 Support and Service

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10 Appendix I: Post Codes

During the boot phase, the BIOS generates a series of status messages (so-called "POST Codes"), which can be output with the help of a suitable reading device (POST Code card). The meanings of the POST Codes are explained in the document "Aptio™ 5.x Status Codes" from American Megatrends®, which is available from the website http://www.ami.com. In addition, the following OEM POST Codes are output:

Code	Description
87h	BIOS-API started
88h	PCA9535 started
89h	PWRCTRL firmware started

11 Appendix II: Resources

11.1 Interrupt

The resources used are independent of the setup setting. The listed interrupts and their use are given by the AT compatibility. If interrupts are to be available only on the ISA side, they must be reserved by the BIOS setup. Exclusivity on the PCI side is neither given nor possible.

11.2 PCI devices

The PCI devices listed here all exist on the board, including those that are detected and configured by the BIOS. Due to the BIOS setup settings it may be the case that various PCI devices or functions of devices are not activated. If devices are deactivated, the bus numbers of other devices may change as a result.

Bus	Dev.	Fct.	Controller / Slot
00	00	00	Host bridge ID 3E30
00	01	00	PCI-to- PCI bridge ID1901
00	01	01	PCI-to- PCI bridge ID1905
00	01	02	PCI-to- PCI bridge ID1909
00	02	00	VGA controller ID3E98
00	08	00	System device ID1911
00	12	00	Data acquisition/signal processing controller ID A379
00	14	00	XHCI USB controller ID A36D
00	14	02	RAM controller ID A36F
00	16	00	Communication device ID A360
00	16	03	Serial device ID A363
00	17	00	RAID controller ID 2822
00	1D	00	PCI-to-PCI bridge ID A330
00	1D	04	PCI-to-PCI bridge ID A334
00	1F	02	ISA bridge ID A306
00	1F	03	HD audio device ID A348
00	1F	04	SMBus controller ID A323
00	1F	05	Controller ID A324
00	1F	06	Ethernet controller ID 15BB
01	00	00	Ethernet controller (PCIE) ID 1533
02	00	00	Ethernet controller (PCIE) ID 1533
03	00	00	Ethernet controller (PCIE) ID 1533

11.3 SMB devices

The following table lists the reserved SM-Bus device addresses in 8-bit notation.

NOTE

These address ranges may not be used by external devices even if the component assigned in the table doesn't exist on the motherboard.

Address	Function
34-35	API access to power supply unit
36-39	Reserved
5C-5D	NCT7491
60-6F	Reserved for DDR4
70-73	POST Code output
88-89	Slave address defined by BIOS
A0-A7	Reserved for DDR4
B0-B3	Power controller (access via BIOS-API)
B8-BB	Power controller (access via BIOS-API)

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